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Application Note

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Specifying Power Consumption

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Power specifications are important to customers, who use the specifications to design their power supplies and thermal solutions. Freescale is a member of the embedded microprocessor benchmark consortium (EEMBC), and uses EEMBC benchmarks for measuring power. This document describes a comparison between the dhrystone benchmark and the EEMBC benchmarks, and briefly looks at I/O power measurements. It includes an analysis of how power measurements are affected by the various features of our devices, and looks at features such as floating point, L2 and L3 caches, AltiVec™, and dynamic power management (DPM). The reviewed devices are PowerPC™ microprocessors.

Contents

1 Dhrystone

Freescale compared typical power measurement uses of EEMBC benchmarks versus power measurements using the dhrystone benchmarks. Dhrystone easily fits on a tester and is representative of the EEMBC benchmarks, which depict real-world applications that Freescale customers might use.

Table 1 shows measurement of average typical power while running the EEMBC benchmarks and measurement of average typical power while running the Dhrystone 2.1

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benchmark on various Freescale processors. The comparison of measurements shows a difference of less than 2 percent, which supports the conclusion that the comparison was very close. Freescale began using the Dhrystone benchmark on testers to measure and specify typical power for Freescale processors.

Table 1. Dhrystone Benchmarks

Source	MPC7410 400MHz 1.8V	MPC7455 800MHz 1.85V	MPC7457 1GHz 1.1V
Average of all EEMBC benchmarks	4.20W	23.08W	7.67W
Dhrystone 2.1	4.30W	23.80W	7.67W
Hardware Spec	4.20W	22.70W	7.50W

2 I/O Power

Earlier, Freescale did not specify I/O power because it depends entirely on the system loading and switching behavior of the outputs, and current of the part to be measured cannot always be isolated from the current of other parts. As a function of capacitive loading, frequency and voltage, I/O power obeys the formula, $P=P_0+CV^2f$.

Worst-case I/O power is difficult to quantify because it involves specifying I/O traffic, which is affected by L2 hit rates, which in turn are dependent on the software. Consequently, Freescale never specified it, but constantly asked about I/O power and decided to attempt to measure it.

2.1 I/O Power Measurements

Figure 1 shows a section of a Valis PMC board for measuring I/O power. To measure I/O power on the OVdd power plane, the resistor R74 is removed from the board and replaced with an ammeter. Completely isolating OVdd was difficult because any current measurements included some additional current from the and buffer. This additional current was very small and did not significantly affect the measurements.

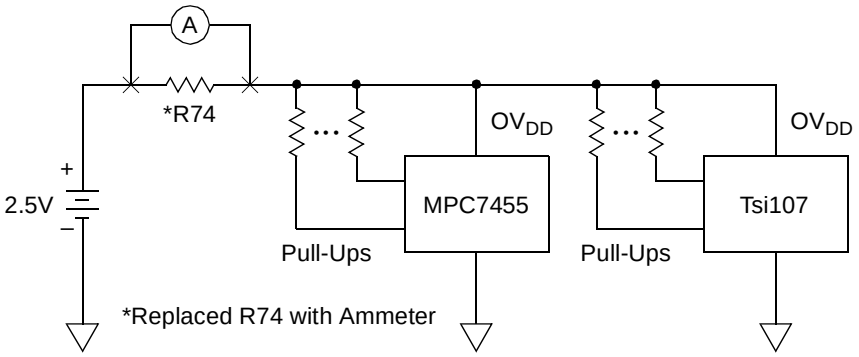

Figure 1. I/O Power Measurement

Taking measurements on a MPC7455 while running each of the 47 EEMBC benchmarks yielded the results that Figure 2 summarizes. The measurements are taken on a 100MHz bus with all the caches disabled to force all signals to be driven on the bus to maximize I/O activity. The I/O power measurements ranged from 236 to 288 mW.

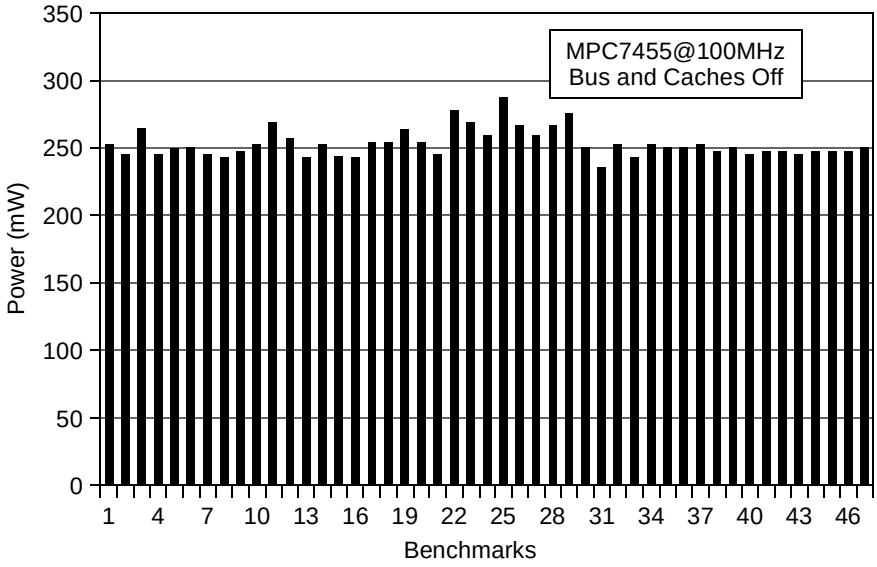

Figure 2. MPC7455 EEMBC Benchmark Results

The average current measured for all 47 benchmarks was 101.5 ma, giving an average I/O power of 253.75 mW. These benchmarks are created to simulate a variety of real world applications. These results represent typical I/O power values for the MPC7455. Typical I/O power values were approximately 250 mW, without much variance.

Sometimes maximum I/O power must be determined to provide enough power supply current. To simulate an application that affects the maximum number of I/O signals as frequently as possible, use the routine depicted in Figure 3.

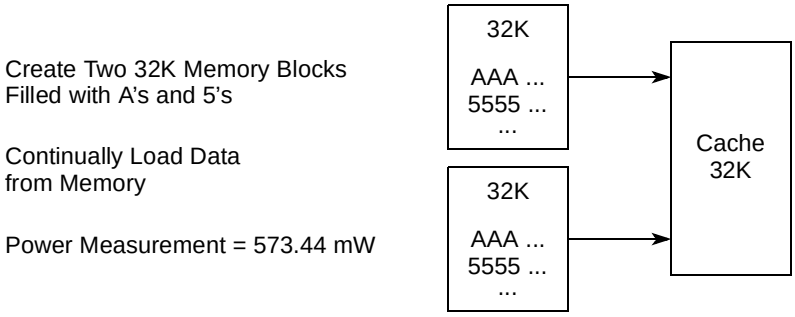

Figure 3. Maximum I/O Power Activity

The routine loads two 32k blocks of memory with alternating lines of 5s and As. In the main loop, it continuously bursts data into the cache, alternating between memory blocks. The size of the memory block is exactly twice the size of the cache to prevent any data from being pulled from the cache instead of memory. The location of the memory blocks was chosen to achieve much variance in address signals. Measuring the power under this condition gave a measurement of 573.44 mW.

2.2 Summary of I/O Power Measurements on Power Dissipation

Although I/O power is not defined in Freescale hardware specifications, the footnotes in the *MPC7410 RISC Microprocessor Hardware Specifications* (MPC7410EC) state that I/O power

<10% of Vdd Power. The MPC745X hardware specifications go a step further in a footnote to state that the values do not include I/O supply power that is system dependent, but is typically <20% of VDD power. For the MPC7455, it is defined typically to be less than 20% of Vdd power. Vdd power is listed in the hardware specification at 17.0 W with a processor frequency of 800 MHz (which is the processor frequency for all examples at 100 MHz bus frequency). This corresponds to a typical I/O power value of 3.4 W. The EEMBC benchmarks simulate typical applications. The I/O power measured was in the range of 250mW, which is less than 2 percent of Vdd power. The maximum value for power measured on the MPC7455 was less than 3 percent of Vdd. These results are summarized in Table 2. According to these results, I/O power as defined in the hardware specification is extremely conservative and can more accurately be described by a smaller value. Beginning with the MPC7457, the specification was revised to say that the I/O power is <5% of VDD power. As earlier specifications are revised, they, too, will show that I/O power is <5% of VDD power.

Table 2. MPC7455 I/O Power Measurements

Source	I/O Measured Power	I/O Power % of V_{DD}
Average of all EEMBC benchmarks	253.75mW	1.2%
Running A's to 5's	573.44mW	2.7%

I/O power is < 3% of V_{DD} power

3 Floating-Point Unit

This section describes the effect of using a floating-point unit on the microprocessor power consumption. The measurements use the EEMBC Bezier Curve benchmark, which has both a fixed point and floating-point version of the same benchmark and allows a direct comparison.

Table 3 displays the results of floating-point analysis. The MPC7410 and MPC7455 show little effect in power consumed when run with floating-point or non-floating-point. The MPC7450 shows a slight decrease in power consumption and the MPC7457 shows a 6.1 percent decrease in power consumption, probably because the integer units are not as busy.

Table 3. Floating Point Effect on Power

Benchmark	Fixed Point	Floating Point	Power Increase
MPC7410 @400 MHz/1.8V using Bezier Curve benchmarks	4.019W	4.015W	.09%
MPC7450 @667 MHz/1.8V using Bezier Curve benchmarks	18.47W	17.99W	–2.3%
MPC7455 @800 MHz/1.85V using Bezier Curve benchmarks	20.83W	20.99W	.7%
MPC7457 @1 GHz/1.1V using Bezier Curve benchmarks	7.33W	6.88W	–6.1%

4 Level 2 Cache

The level 2 cache test describes the effect of using the L2 cache on power consumption while running 45 of the EEMBC benchmarks shown in Table 4. The light colored bars represent running the benchmark with the L2 off; dark colored bars represent L2 on.

Table 4. EEMBC Benchmarks Applied to MPC7410 and MPC7450 L2 Cache Test

Benchmark Number	Benchmark Name
1	Angle-to-Time Conversion
2	FFT - Fast Fourier Transform
3	FIR - Finite Impulse Response Filter
4	iFFT - inverse Fast Fourier Transform
5	Basic Integer & Floating Point
6	Bit Manipulation
7	Cache Buster
8	CAN Remote Data Request
9	iDCT- inverse Discrete Cosine Transform
10	IIR - Infinite Impulse Response
11	Matrix Arithmetic
12	Pointer-Chasing
13	Pulse-Width Modulation
14	Road Speed Calculation
15	Table Lookup and Interpolation
16	Tooth-to-Spark
17	JPEG-compress
18	JPEG-decompress
19	High Pass Grey-scale Filter
20	RGB to CYMK Conversion
21	RGB to YIQ Conversion
22	OSPF/Dijkstra
23	Packet Flow
24	Packet Flow
25	Packet Flow
26	Route lookup
29	Dithering (Floyd-Steinberg)
28	Image Rotation
29	Text Processing
30	Auto-Correlation (DATA_2: rsine.dat 16)
31	Auto-Correlation (DATA_3: rspeech.dat 32)
32	Auto-Correlation (DATA_1: rpulse.dat 8)
33	Convolutional Encoder (DATA_3: rk3r2.dat 1)
34	Convolutional Encoder (DATA_1: rk5r2.dat 3)

Table 4. EEMBC Benchmarks Applied to MPC7410 and MPC7450 L2 Cache Test (continued)

Benchmark Number	Benchmark Name
35	Convolutional Encoder (DATA_2: rk4r2.dat 2)
36	Fixed Point Bit Allocation (DATA_6: rpent.dat 500)
37	Fixed Point Bit Allocation (DATA_3: rstep.dat 120)
38	Fixed Point Bit Allocation (DATA_2: rtyp.dat 120)
39	Fixed Point Complex FFT/IFFT (DATA_3:rsin.dat f)
40	Fixed Point Complex FFT/IFFT (DATA_1:rpul.dat f)
41	Fixed Point Complex FFT/IFFT (DATA_2:rspn.dat f)
42	Viterbi Decoder (DATA_4: rzerost.dat 4)
43	Viterbi Decoder (DATA_1: rgeti.dat 1)
44	Viterbi Decoder (DATA_2: rtogglet.dat 3)
45	Viterbi Decoder (DATA_3: ronest.dat 2)

4.1 MPC7410 Level 2 Cache

Figure 4 shows the results of running the suite of benchmarks on the MPC7410 at 400 MHz and 1.8 V core V_{dd}. Activating the L2 slightly increases power. The largest increases in power are shown in the matrix arithmetic benchmark (11) and RGB-to-CYMK color conversion benchmark (20) with increases of 4 percent and 5 percent, respectively. The average typical power with the L2 is 4.35 W.

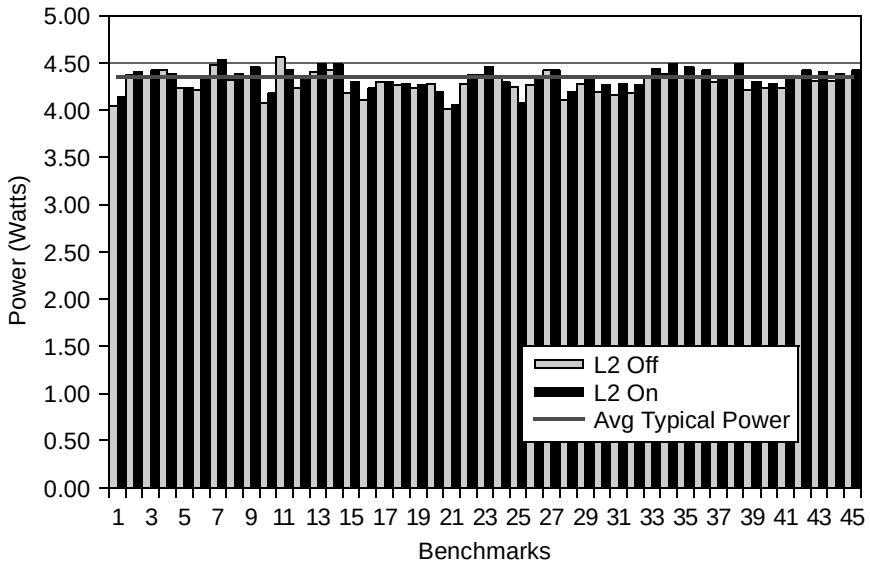

Figure 4. MPC7410 L2 Cache at 400MHz/1.8V

4.2 MPC7455 Level 2 Cache

Figure 5 shows the results of running the suite of benchmarks on the MPC7455 at 1GHz and 1.85 V. Overall, power increases slightly. The average typical power with the L2 is 23.83 W. The largest increases

are shown in packet flow (25), which had a 13 percent increase in power consumption for a 2-Mbyte cache.

The biggest effect in a suite was in the consumer suite, where the JPEG compress and JPEG decompress benchmarks (17–18) had a power increase of 5.5 percent and the two RGB color conversion benchmarks (20–21) showed a 7 percent increase in power. The average typical power with the L2 is 23.83 W.

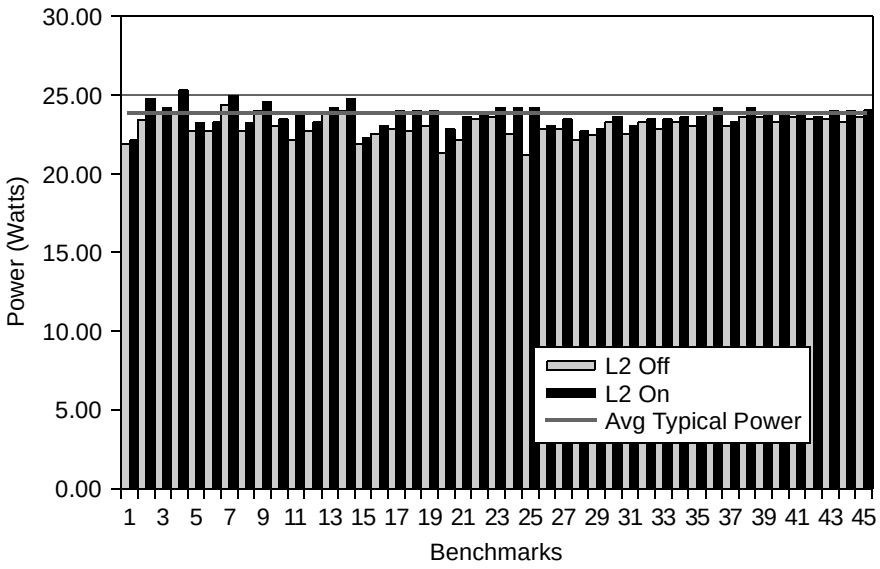

Figure 5. MPC7455 L2 Power Measurements at 800MHz/1.85V

4.3 MPC7457 Level 2 Cache

Figure 6 shows results of running the suite of 47 EEMBC benchmarks as shown in Table 5 on the MPC7457. Again, power increases slightly. The largest increases are shown in packet flow (25), which had a 12% increase in power consumption when using a 2-Mbyte buffer size. The biggest effect in a suite was in the consumer suite, where the JPEG compress and JPEG decompress benchmarks (17–18) had a power increase of 6% and the two RGB color conversion benchmarks (20–21) showed a 7 percent increase in power. The average typical power with the L2 on is 7.67 W.

Table 5. EEMBC Benchmarks Applied to MPC7457 Level2 Cache Test

Benchmark Number	Benchmark Name
1	Angle-to-Time Conversion
2	Basic Integer & Floating Point
3	Bit Manipulation
4	Cache Buster
5	CAN Remote Data Request
6	FFT - Fast Fourier Transform
7	FIR - Finite Impulse Response Filter
8	IIR - Infinite Impulse Response

Table 5. EEMBC Benchmarks Applied to MPC7457 Level2 Cache Test (continued)

Benchmark Number	Benchmark Name
9	iDCT- inverse Discrete Cosine Transform
10	iFFT - inverse Fast Fourier Transform
11	Matrix Arithmetic
12	Pointer-Chasing
13	Pulse-Width Modulation
14	Road Speed Calculation
15	Table Lookup and Interpolation
16	Tooth-to-Spark
17	JPEG-compress
18	JPEG-decompress
19	High Pass Grey-scale Filter
20	RGB to CYMK Conversion
21	RGB to YIQ Conversion
22	Auto-Correlation (DATA_2: rsine.dat 16)
23	Auto-Correlation (DATA_3: rspeech.dat 32)
24	Auto-Correlation (DATA_1: rpulse.dat 8)
25	Convolutional Encoder (DATA_3: rk3r2.dat 1)
26	Convolutional Encoder (DATA_1: rk5r2.dat 3)
27	Convolutional Encoder (DATA_2: rk4r2.dat 2)
28	Fixed Point Bit Allocation (DATA_6: rpent.dat 500)
29	Fixed Point Bit Allocation (DATA_3: rstep.dat 120)
30	Fixed Point Bit Allocation (DATA_2: rtyp.dat 120)
31	Fixed Point Complex FFT/IFFT (DATA_3:rsin.dat f)
32	Fixed Point Complex FFT/IFFT (DATA_1:rpul.dat f)
33	Fixed Point Complex FFT/IFFT (DATA_2:rspn.dat f)
34	Viterbi Decoder (DATA_4: rzerost.dat 4)
35	Viterbi Decoder (DATA_1: rgeti.dat 1)
36	Viterbi Decoder (DATA_2: rtogglet.dat 3)
37	Viterbi Decoder (DATA_3: ronest.dat 2)
38	OSPF/Dijkstra
39	Route lookup
40	Packet Flow
41	Packet Flow

Table 5. EEMBC Benchmarks Applied to MPC7457 Level2 Cache Test (continued)

Benchmark Number	Benchmark Name
42	Packet Flow
43	Bezier Curves (Fixed)
44	Bezier Curves (Float)
45	Dithering (Floyd-Steinberg)
46	Image Rotation
47	Text Processing

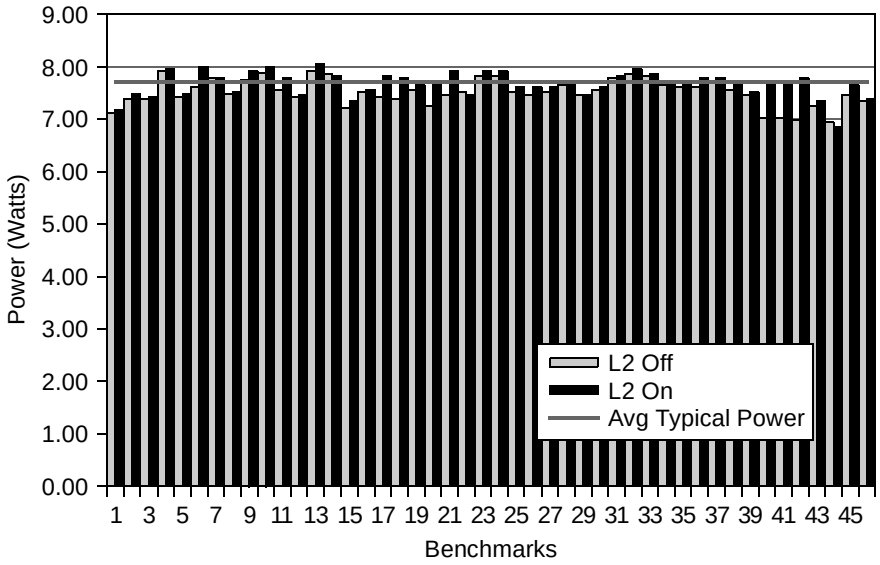

Figure 6. MPC7457 L2 Power Measurements at 1GHz/1.1V

4.4 Summary of L2 Cache Effect on Power Dissipation

Table 6 displays the results of the L2 cache power analysis. On all the EEMBC benchmarks, the MPC7410 showed just a slight increase of power when the L2 was used. The effect on the MPC7455 and MPC7457 was greater but still quite small with increases of just 3.1 percent and 2 percent in power.

Table 6. Cache Effect on Power

Benchmark	Without L2	With L2	Power Increase
MPC7410 @400MHz/1.8V using EEMBC benchmarks	4.29W	4.35W	1.4%
MPC7455 @800MHz/1.85V using EEMBC benchmarks	23.11W	23.83W	3.1%
MPC7457 @1GHz/1.1V using EEMBC benchmarks	7.52W	7.67W	2.0%

5 Level 3 Cache

The level 3 cache test describes the effect of using the L3 cache on power consumption while running all of the EEMBC benchmarks shown in Table 4 for the MPC7455 and in Table 5 for the MPC7457. The L3 cached was turned on and a power measure was taken to measure power increase caused by on-chip tags. The light-colored bars represent running the benchmark with the L3 off; the dark-colored bars represent the L3 on.

5.1 MPC7455 Level 3 Cache

Figure 7 shows results of running the suite of benchmarks shown in Table 4 on the MPC7455. The L3 power consumption on an MPC7455 running at a core frequency of 1GHz, 1.6V core V_{dd}, an L3 frequency of 266Mhz was measured with an operating junction temperature of 65°C with the L3 cache turned on. Power consumption increased slightly. The average typical power with L3 engaged is 21.67W.

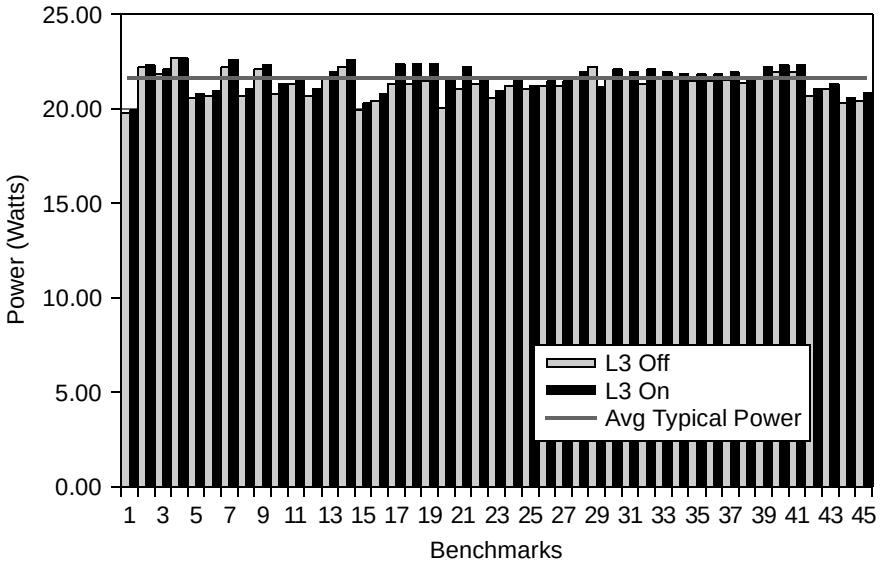

Figure 7. MPC7455 L3 Power Measurements at 1GHz/1.6V

5.2 MPC7457 Level 3 Cache

Figure 8 shows results of running the suite of benchmarks shown in Table 7 on page 11 on the MPC7457. The L3 power consumption on an MPC7457 running at a core frequency of 1 GHz, core V_{dd} of 1.1V, L3 frequency of 266 MHz was measured with an operating junction temperature of 65°C with the L3 cache turned on. Power consumption increased slightly. The average typical power with L3 engaged is 7.7 W.

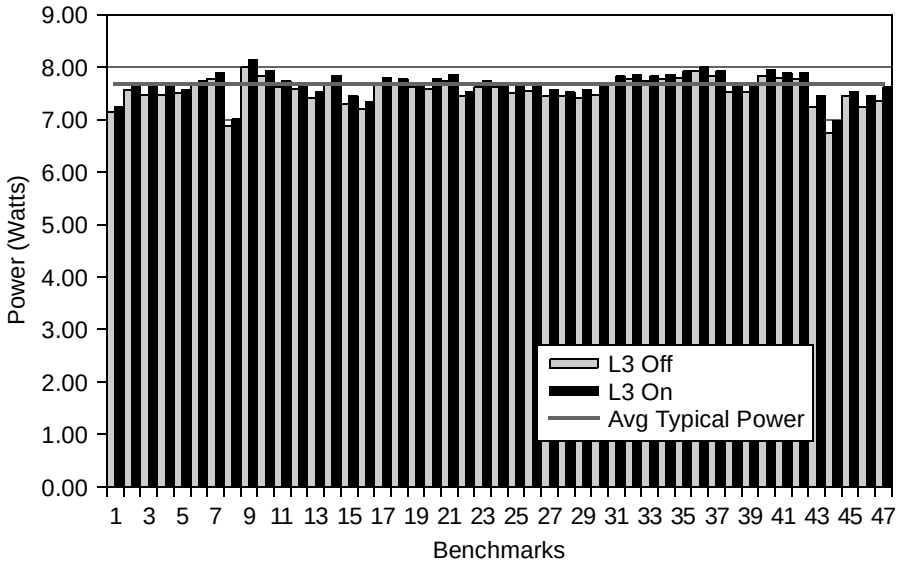

Figure 8. MPC7457 L3 Power Measurements at 1GHz/1.1V

5.3 Summary of L3 Cache Effect on Power Dissipation

Table 7 displays the results of the L3 cache power analysis. When averaging all of the EEMBC benchmarks, an average increase of 1.85% with the use of the L3 Cache on the MPC7455 and an 1.64% increase of power on the MPC7457 occurred.

Table 7. L3 Cache Effect on Power

Benchmark	Without L3	With L3	Power Increase
MPC7455 @800MHz/1.85V using all EEMBC benchmarks	21.27W	21.67W	1.85%
MPC7457 @1GHz/1.1V using all EEMBC benchmarks	7.58W	7.70W	1.64%

6 AltiVec

This section describes the effect of the AltiVec technology unit on power consumption. AltiVec is supported on PowerPC microprocessors such as the MPC7410, MPC7451, MPC7455, and MPC7457. These measurements were taken from 14 vectorized benchmarks from the Telecommunications and Networking suite of EEMBC benchmarks shown in Table 8. Measurements were taken initially while running benchmarks that EEMBC provided out of the box. Then the benchmarks were rewritten (vectorized) to take advantage of AltiVec technology.

Table 8. EEMBC Vectorized Benchmarks

Benchmark Number	Benchmark Name
1	Packet Flow
2	Packet Flow
3	Packet Flow
4	Route Lookup

Table 8. EEMBC Vectorized Benchmarks (continued)

Benchmark Number	Benchmark Name
5	Convolutional Encoder (DATA_3: rk3r2.dat 1)
6	Convolutional Encoder (DATA_1: rk5r2.dat 3)
7	Convolutional Encoder (DATA_2: rk4r2.dat 2)
8	Fixed Point Complex FFT/IFFT (DATA_3:rsin.dat f)
9	Fixed Point Complex FFT/IFFT (DATA_1:rpul.dat f)
10	Fixed Point Complex FFT/IFFT (DATA_2:rspn.dat f)
11	Viterbi Decoder (DATA_4: rzerost.dat 4)
12	Viterbi Decoder (DATA_1: rgeti.dat 1)
13	Viterbi Decoder (DATA_2: rtogglet.dat 3)
14	Viterbi Decoder (DATA_3: ronest.dat 2)

6.1 MPC7410 AltiVec

Figure 9 shows results of running the vectorized benchmarks from the Networking and Telecommunication suites of EEMBC benchmarks on the MPC7410 at 400MHz and 1.8V. Freescale ran the EEMBC benchmarks and then recoded the benchmarks to take advantage of AltiVec technology. With AltiVec, power increased overall, and the greatest increase in power consumption, 13-16%, occurred during the vectorized Viterbi Decoder benchmarks(11-14).

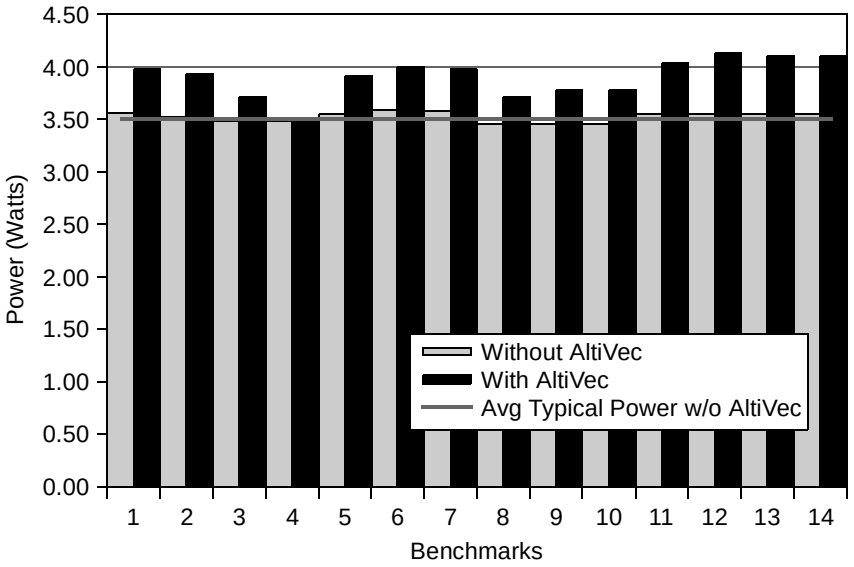

Figure 9. MPC7410 AltiVec Power Measurements at 400 MHz/1.8V

6.2 MPC7455 AltiVec

Figure 10 shows results of running 14 vectorized benchmarks on the MPC7455 at 800 MHz and 1.85 V. Again the greatest increase in power consumption (12–13%) occurred when running some of the vectorized Viterbi Decoder benchmarks (13–15), which are computationally extensive.

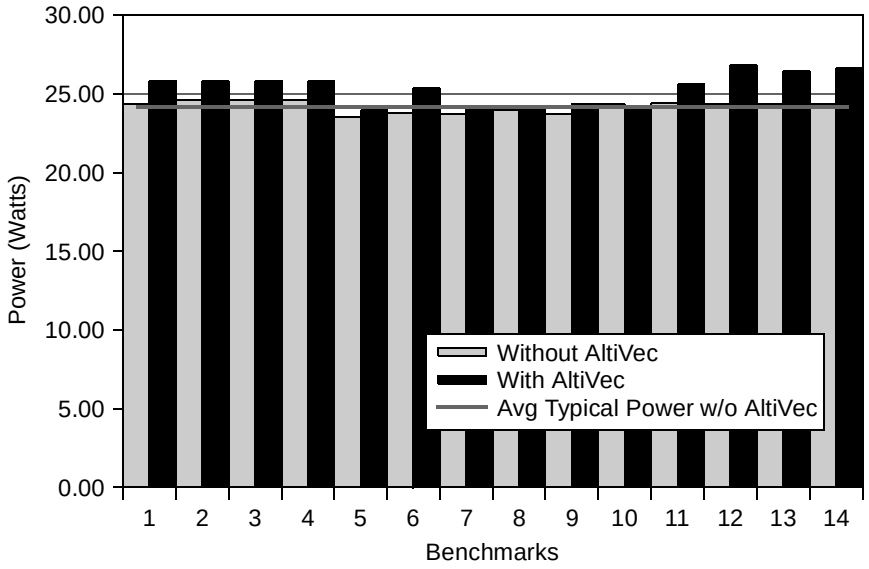

Figure 10. MPC7455 AltiVec Power Measurements at 800MHz/1.85V

6.3 MPC7457 AltiVec

Figure 11 shows results for the MPC7457 at 1 GHz and 1.1 V. When testing this device, Freescale ran more benchmarks (20), as Table 9 shows. Power consumption increased, and the greatest increase, which as 7–10 percent, occurred when running some of the vectorized Viterbi Decoder benchmarks (13–16).

Table 9. MPC7457 AltiVec Benchmarks

Benchmark Number	Benchmark Name
1	Auto-Correlation
2	Auto-Correlation
3	Auto-Correlation
4	Convolutional Encoder
5	Convolutional Encoder
6	Convolutional Encoder
7	Fixed Point Bit Allocation
8	Fixed Point Bit Allocation
9	Fixed Point Bit Allocation
10	Fixed Point Complex FFT/IFFT
11	Fixed Point Complex FFT/IFFT
12	Fixed Point Complex FFT/IFFT
13	Viterbi Decoder
14	Viterbi Decoder
15	Viterbi Decoder

Table 9. MPC7457 AltiVec Benchmarks

Benchmark Number	Benchmark Name
16	Viterbi Decoder
17	Route lookup
18	Packet Flow
19	Packet Flow
20	Packet Flow

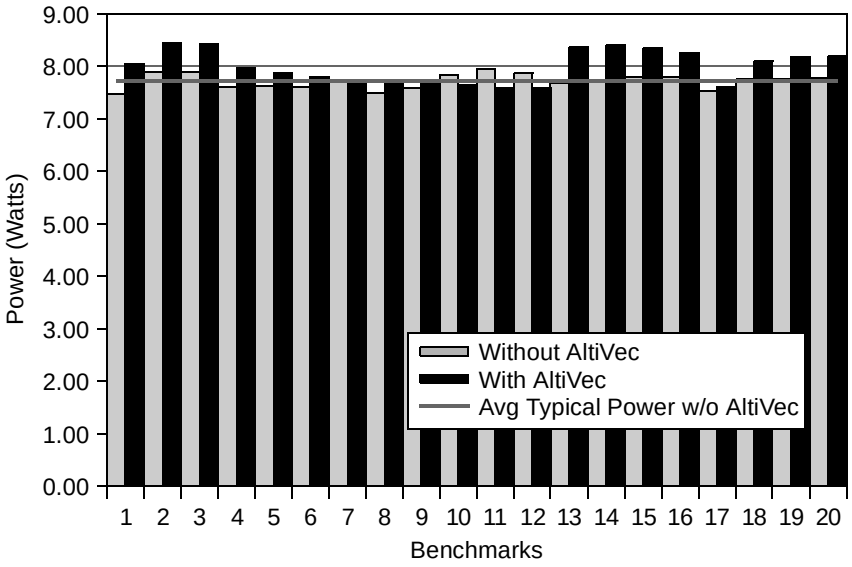

Figure 11. MPC7457 AltiVec Power Measurements at 1GHz and 1.1V

6.4 AltiVec Performance Improvement

Of all the features examined, the AltiVec feature gave the largest power increase. Therefore, is it worth using AltiVec. Freescale analyzed the kind of performance improvement for the increase in power consumption and measured performance by counting the iterations per second to run the benchmarks with and without AltiVec.

6.4.1 MPC7410 AltiVec Performance

Figure 12 shows the performance results for the MPC7410 when 14 different benchmarks were run from the Networking and Telecommunication suites of The EEMBC benchmarks that had been coded for AltiVec. The largest gain, a 22–36X increase in performance, occurred on the Convolutional Encoder benchmarks. The geometric mean of the gains are shown in a suite because EEMBC reports results in that manner. The geometric mean of these gains yields an increase of 3.86X for the Networking benchmarks and 6.88X for the Telecommunication benchmarks.

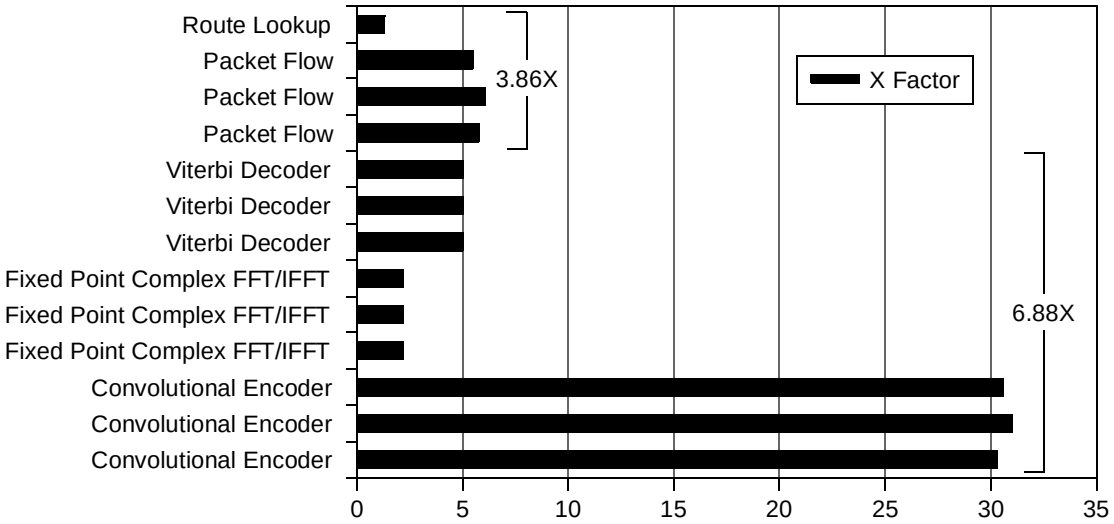

Figure 12. MPC7410 AltiVec Performance Improvement

6.4.2 MPC7455 AltiVec Performance

Figure 13 shows results of using AltiVec on the MPC7455. The largest gain is on the Convolutional Encoder benchmarks, with a 27-34X increase in performance. Taking the geometric mean of these gains by suite shows an increase of 3.7X for the Networking benchmarks and 6.3X for the Telecommunications benchmarks.

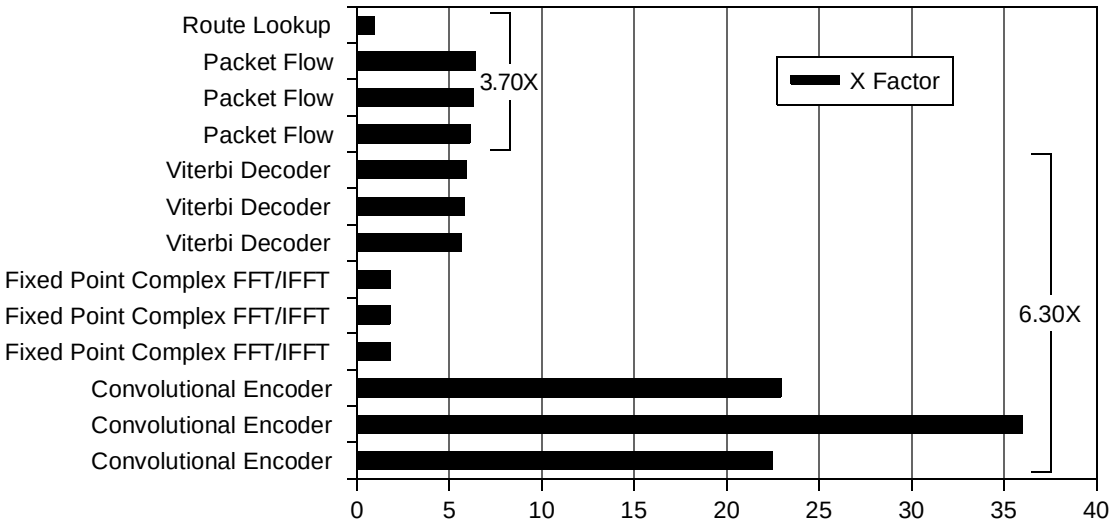

Figure 13. MPC7455 AltiVec Performance Improvement

6.4.3 MPC7457 AltiVec Performance

Figure 14 shows results of using AltiVec on the MPC7457. When measuring the MPC7457, Freescale used 20 benchmarks in the Networking and Telecommunication suites of The EEMBC benchmarks. The largest gain is on the Convolutional Encoder benchmarks(5-7) with a 34X increase in performance. Taking the geometric mean of these gains yields an increase of 3.287X for the Networking benchmarks and 4.35X for the Telecommunications benchmarks.

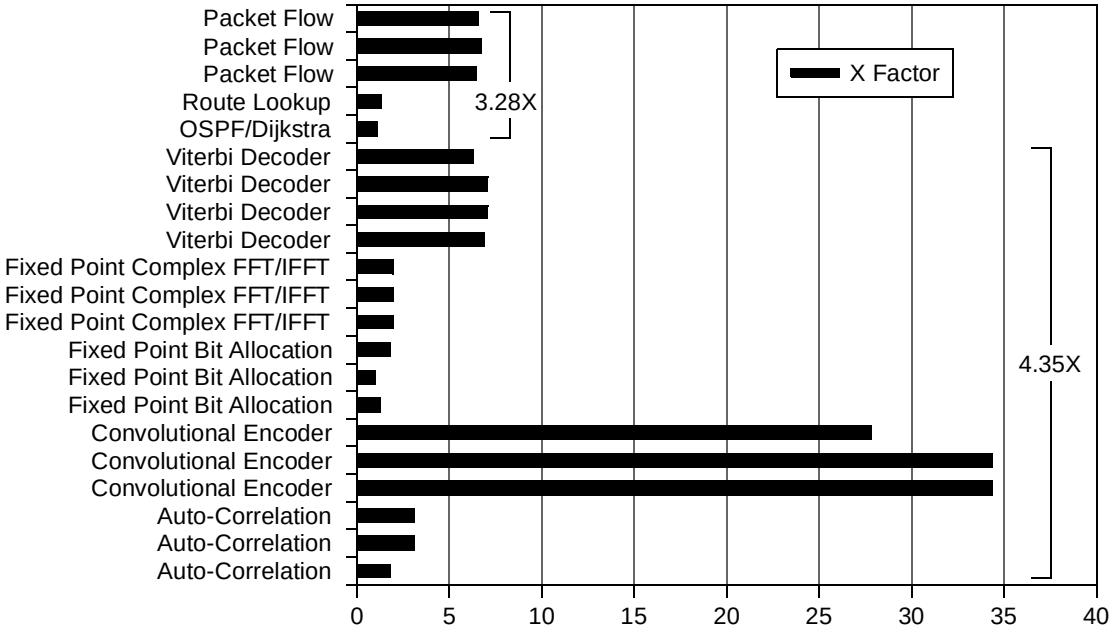

Figure 14. MPC7457 AltiVec Performance Improvement

6.5 Summary of AltiVec on Power Dissipation

Table 10 displays the results on power consumption when using an Altivec unit. The results of using AltiVec on EEMBC benchmarks show that for a 4-11% increase in power consumption a 4-6X performance improvement is gained.

Table 10. AltiVec Effect on Power

Benchmark	AltiVec Off	AltiVec On	Power Increase	Performance Improvement
MPC7410 @400MHz/1.8V using 14 EEMBC benchmarks	3.51W	3.88W	10.75%	5.76X
MPC7455 @800MHz/1.85V using 14 EEMBC benchmarks	24.27W	25.43W	4.75%	5.40X
MPC7457 @1GHz/1.1V using 20 EEMBC benchmarks	7.72W	8.00W	4.5%	4.07X

7 Dynamic Power Management

This section details the effect of using Dynamic Power Management (DPM) on power consumption. The light-colored bars represents running the benchmark with the DPM off and the dark- colored bars with the DPM on.

7.1 MPC7410 Dynamic Power Management

Figure 15 shows results of running 45 EEMBC benchmarks shown in Table 4 on the MPC7410 at 400MHz and 1.8V. The results show a decrease in power consumption with the use of Dynamic Power Management.

The effect of not using DPM is most noticeable in the Auto/Industrial suite of EEMBC, with the Table Lookup and Interpolation (15) and Tooth to Spark (16) benchmarks showing 3.5 to 4% increases in power consumption.

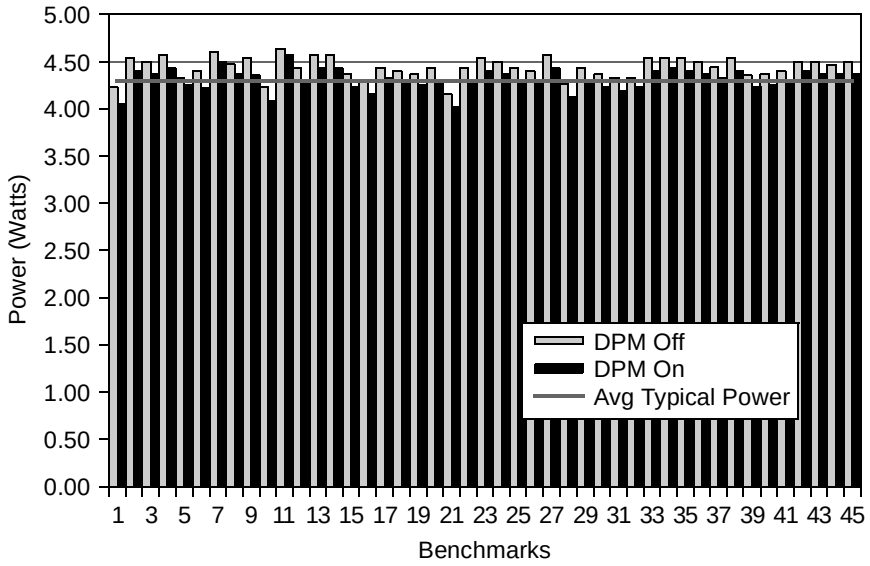

Figure 15. MPC7410 DPM Measurements at 400MHz/1.8V

7.2 MPC7455 Dynamic Power Management

Figure 16 shows results of running 45 EEMBC benchmarks shown in Table 4 on page 5 on the MPC7455 at 1GHz and 1.85V. The greatest effect was seen in the Telecommunications suite of EEMBC benchmarks with the Auto Correlation benchmarks (30-32), showing 7-8% increases in power consumption when testing without Dynamic Power Management.

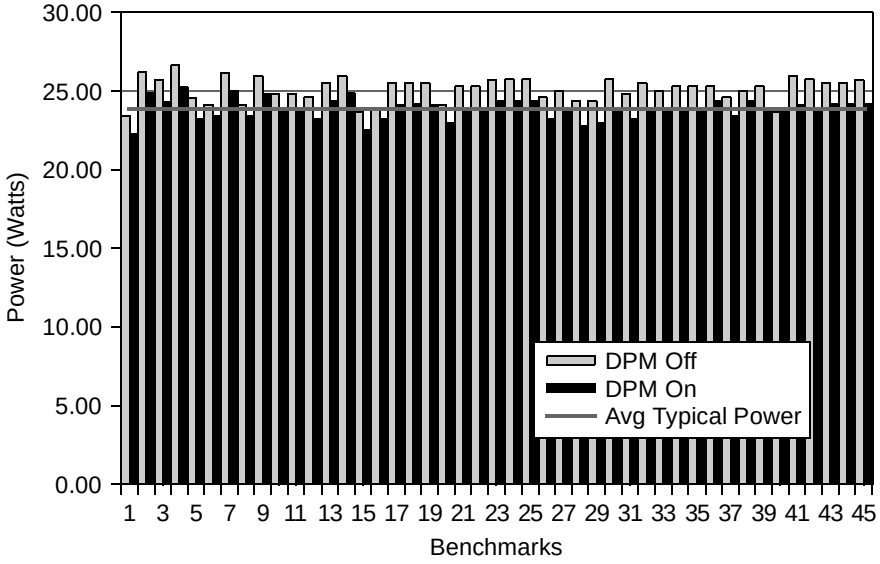

Figure 16. MPC7455 DPM Power Measurements at 800MHz/1.85V

7.3 MPC7457 Dynamic Power Management

Figure 17 shows results of running 47 EEMBC benchmarks as shown in Table 5 on page 7 on the MPC7457 at 1GHz and 1.1V. When testing without Dynamic Power Management, in every case a power increase occurred. Increases ranged from 4–9 percent.

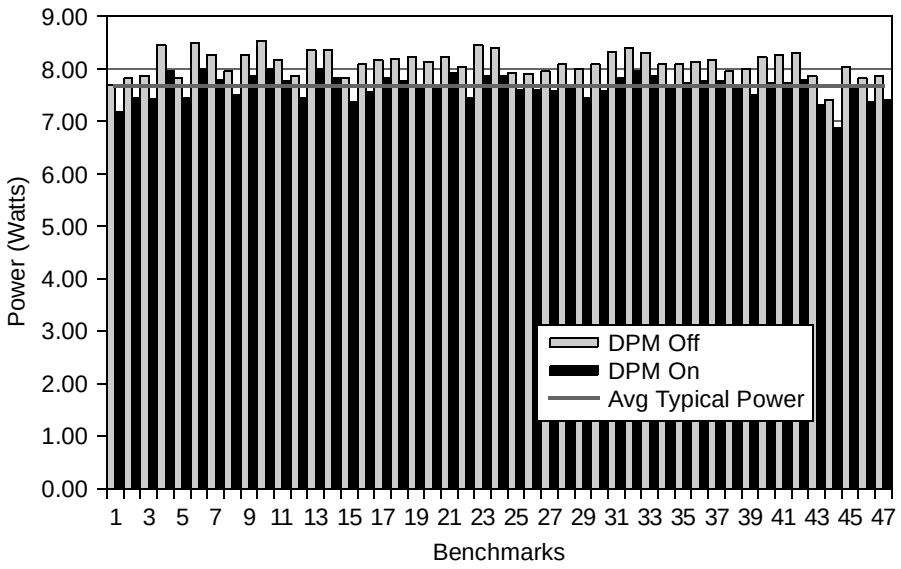

Figure 17. MPC7457 DPM Power Measurements at 1 GHz/1.1V

7.4 Summary of Dynamic Power Management on Power Dissipation

Table 11 shows results of the analysis of power consumption for dynamic power management. Results of averaging all EEMBC benchmarks that were run show power savings of about 3 percent on the MPC7410 and about 6 percent on the MPC7455 and MPC7457 when using dynamic power management. Freescale recommends that customers consistently use dynamic power management.

Table 11. DPM Effect on Power

Benchmark	DPM Off	DPM In	Power Increase
MPC7410 @ 400 MHz/1.8V using EEMBC benchmarks	4.30 W	4.18 W	–2.8%
MPC7455 @ 800 MHz/1.85V using EEMBC benchmarks	23.45 W	22.14 W	–5.6%
MPC7457 @ 1 GHz/1.1V using EEMBC benchmarks	8.12 W	7.67 W	–5.5%

7.4.1 Commentary on Measuring Typical Power

Figure 18 shows a graph of continuous measurement of typical power with all 47 EEMBC benchmarks running on a MPC7457 at 1GHz frequency, 1.1 V, and 65° C. Each peak represents a different benchmark. Notice that the device at rest dissipates just under 6 W. As the benchmarks are loading and unloading, the power registers around 6.2 W, and when the benchmarks are running, some of them go as high as 7.4 W. We spec typical power based upon the average of the maximum power of the peaks. The typical power measurement for the MPC7457 device measures 7.01 W, which is represented by the top straight line. An average power reading of this device for the whole period in which these benchmarks ran is 6.27 W, which is represented by the lower straight line on the graph. This analysis indicates that some margin may exist

in Freescale specifications of power numbers, depending on the customer application. For normal use, the device is occasionally not at peak activity, and the customer's power plots over time may look just like the plot in Figure 18.

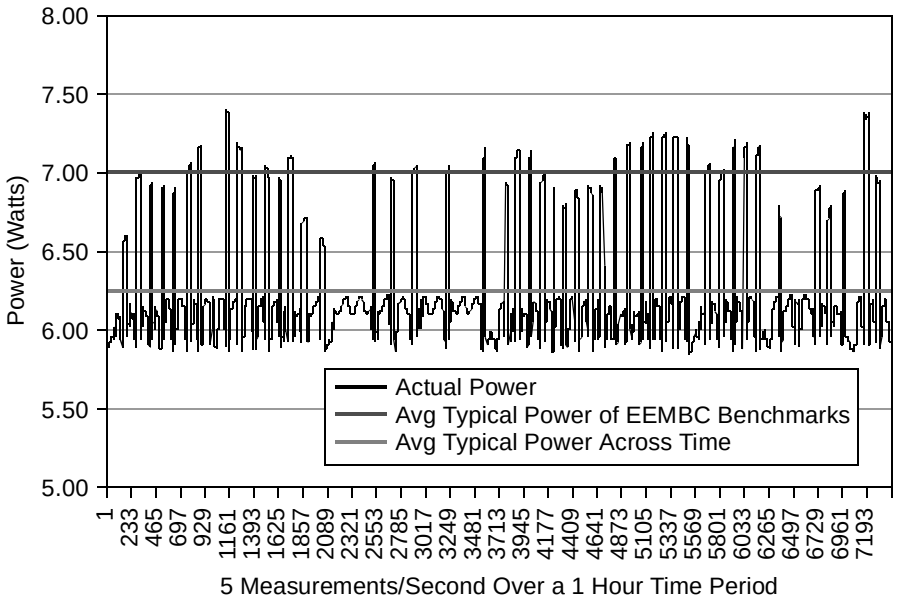

Figure 18. Power During Complete Run of EEMBC Benchmarks on MPC7457 at 1GHz/1.1V/65°C

8 Conclusions

Freescale drew the following conclusions after thorough testing:

- The dhrystone benchmark compares well as a benchmarking measurement and can easily be used on our production testers to measure and specify typical power.
- Previous predictions of I/O power were inaccurate; I/O power is less than 3% of Vdd power.
- After looking at the effects of the various features of select microprocessors on the devices' power consumption, Freescale concludes that power consumption impacts are minor when running devices with or without the features activated.
- AltiVec technology gives a 4-6X performance boost for a small increase in power.

9 Revision History

Table 12 shows the revision history of this document.

Table 12. Revision History

Revision Number	Changes
0.0	Initial release
0.1	Nontechnical reformatting
2	Nontechnical reformatting

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