

AN14071

Trace Implementation on i.MX RT1170

Rev. 1 — 13 November 2023

Application note

Document information

Information	Content
Keywords	AN14071, Trace implementation, i.MX RT1170
Abstract	This document describes the trace implementation by different probe and IDE on the i.MX RT1170 EVK.



1 Introduction

This document describes the trace implementation by different probe and IDE on the i.MX RT1170 EVK. [Table 1](#) lists the trace mode, IDE, and probe cases discussed in this document.

Table 1. Topics for discussion

Serial Wire Output (SWO)/Embedded Trace Macrocell (ETM) trace	IDE	Probe
SWO trace	MCUXpresso	On board LPCLINK2-J-Link
SWO trace	IAR	On board LPCLINK2-J-Link
SWO trace	KEIL	On board LPCLINK2-J-Link
SWO trace	MCUXpresso	J-Link
SWO trace	IAR	J-Link
SWO trace	KEIL	J-Link
SWO trace	TRACE32	uTRACE
ETM trace	Ozone	J-Trace
ETM trace	TRACE32	uTRACE

The IDE version used for this application note is:

- MCUXpresso: V11.8.0
- IAR: V9.40.1
- KEIL: V5.37.0.0

The board used in this application note is:

- MIMXRT1170-EVK SCH-32171 REVC

2 Implementation

This section describes the SWO trace and ETM trace implementation.

2.1 SWO trace by onboard LPCLink2 J-Link

Below describes the SWO trace by onboard LPCLink2 J-Link.

2.1.1 Board setup for LPCLink2 J-Link

This section describes the board setup for LPCLink2 J-Link.

2.1.1.1 Enable LPCLINK2 J-Link on i.MX RT1170 EVK

The default probe firmware on the i.MX RT1170 EVK board is DAPLink CMSIS DAP, which does not support the SWO trace. So, we need to switch to LPCLink2 J-Link.

To switch to LPCLink2 J-Link, follow the steps below:

1. Download LPCScript from <https://www.nxp.com/lpcscript> and install it.
2. Install the jumper J22 (Marked in [Figure 1](#)) and connect the USB cable.

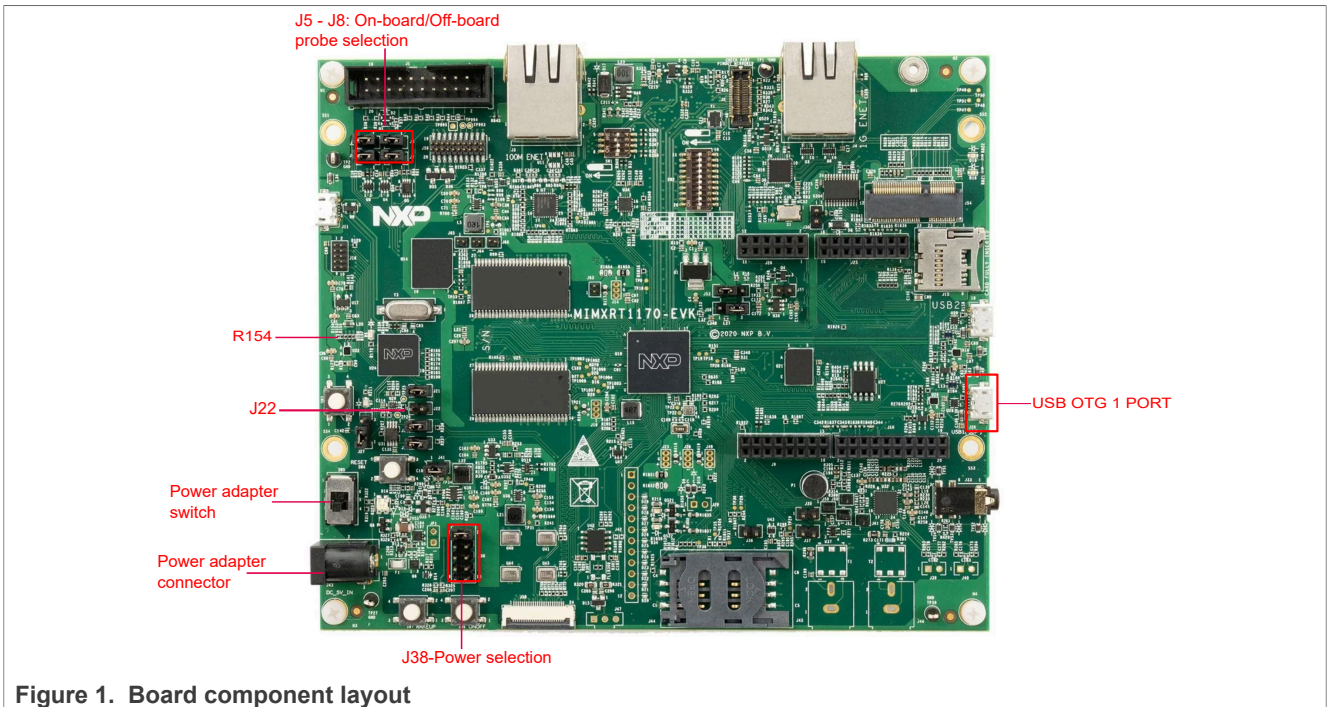


Figure 1. Board component layout

3. Run the program LPC-Link2 with Segger J-Link from the Windows **Start** menu.

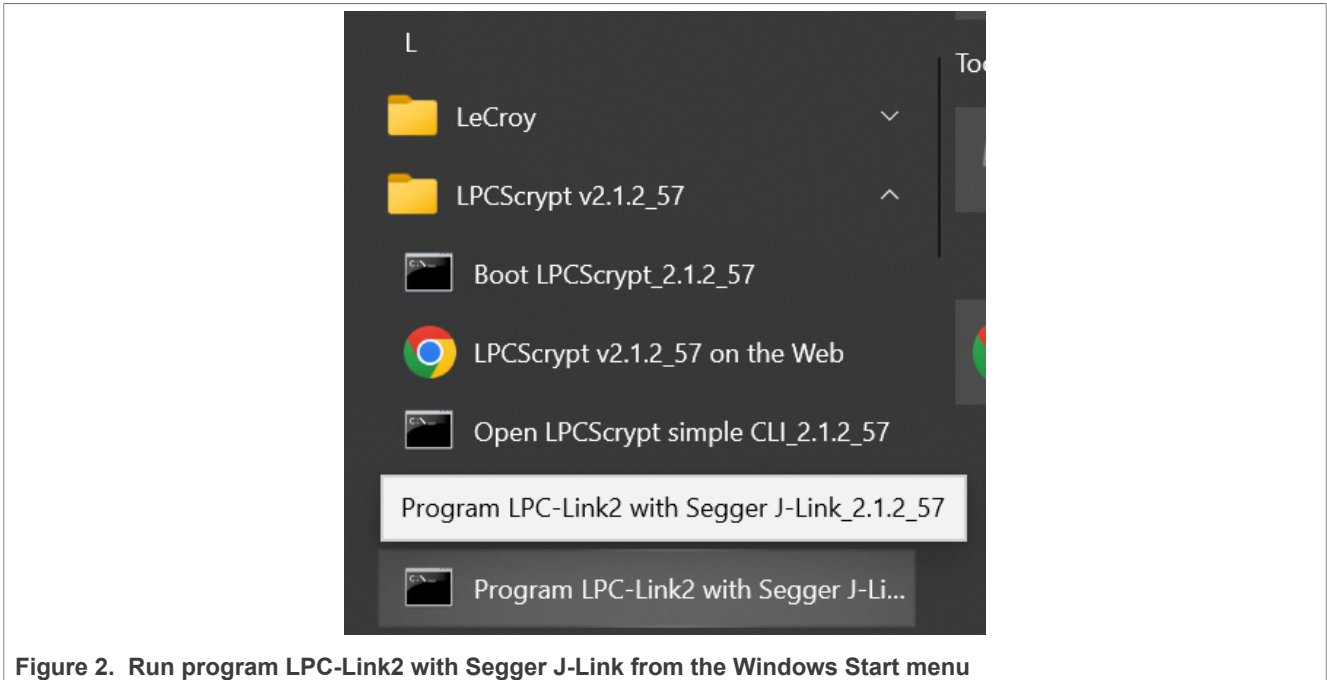


Figure 2. Run program LPC-Link2 with Segger J-Link from the Windows **Start** menu

4. To program LPCLink2 J-Link, press the Enter key and the log is as shown in [Figure 2](#).

```

C:\Program Files\Segger\J-Link>V2.1.2_57 - C:\NXP\LPCScript_2.1.2_57\scripts\program_JLINK.cmd
LPCScript - J-Link firmware programming script v2.1.2 Nov 2020.

Connect an LPC-Link2 or LPCXpresso V2/V3 Board via USB then press Space.

Press any key to continue . . .

Booting LPCScript target with "LPCScript_240.bin.hdr"
LPCScript target booted

Programming LPCXpresso V2/V3 with "Firmware_JLink_LPCXpressoV2_20190404.bin"

LPCXpresso V2/V3 programmed successfully:
- To use: remove DFU link and reboot.

Connect Next Board then press Space (or CTRL-C to Quit)

Press any key to continue . . .
    
```

Figure 3. Program LPCLink2 J-Link

5. Disconnect jumper J22 and reconnect the USB cable. Now, the board is seen not powered. It is a known issue in LPCScript v2.1.2. To solve this issue, there are three possible workarounds. Apply one of the following steps:
 - a. Change the connection to be 1 - 2 on J38 (marked in [Figure 1](#)), and power the board by a power adapter.
 - b. Change the connection to be 3 - 4 on J38 (marked in [Figure 1](#)), and power the board by USB OTG1 port (marked in [Figure 1](#)).
 - c. Solder R154 (marked in [Figure 1](#)), and power the board by USB debug port.
 Then, the board can be powered.

2.1.1.2 Jumper settings

Connect J5, J6, J7, and J8 (marked in [Figure 1](#)) to select LPCLink2 J-Link.

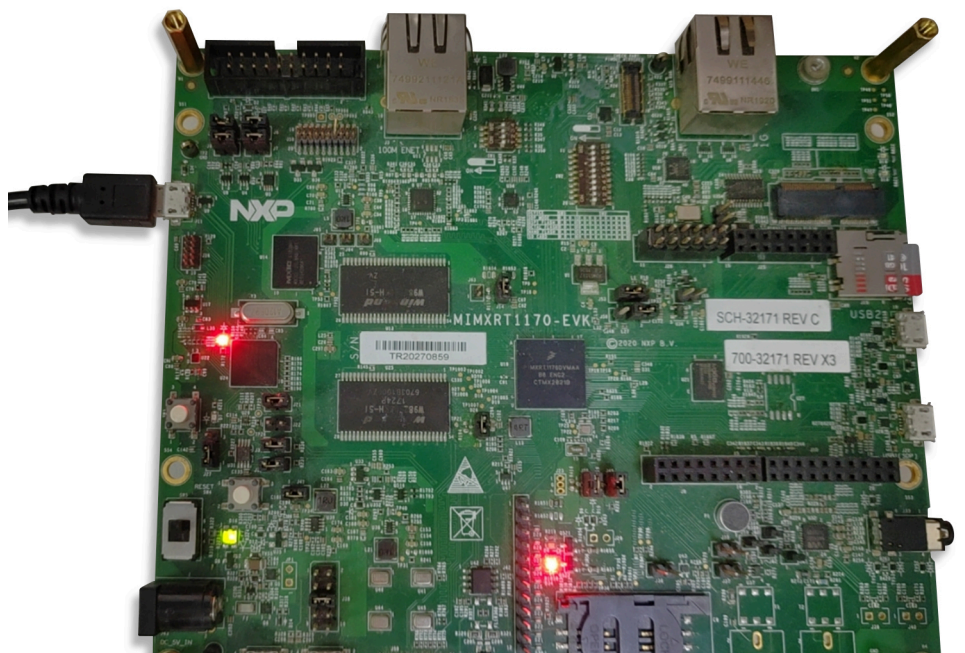


Figure 4. Board setup for LPCLink2 J-Link

2.1.2 By MCUXpresso

To set up the board for LPCLink2-J-Link, see [Section 2.1.1](#) first.

1. Unzip and import the project `evkmimxrt1170_swo_demo_cm7_mcuxpresso` in AN14071SW. Build and start debugging.
2. Build and run the code, when it stops at `main()`. Configure the clock. Click the **Change** button.

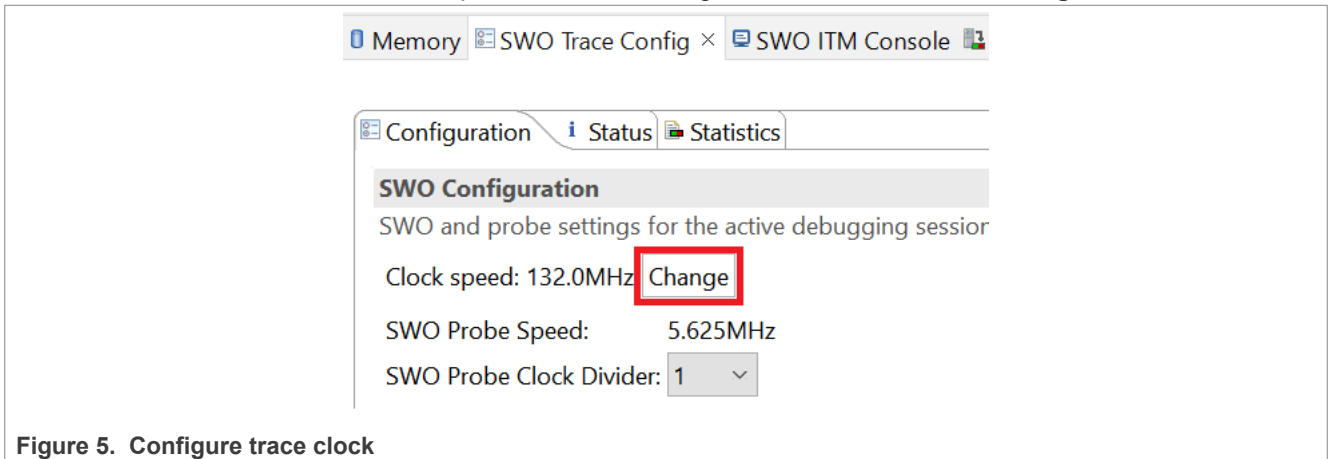


Figure 5. Configure trace clock

Then set the core and trace the clock, as shown in [Figure 6](#).

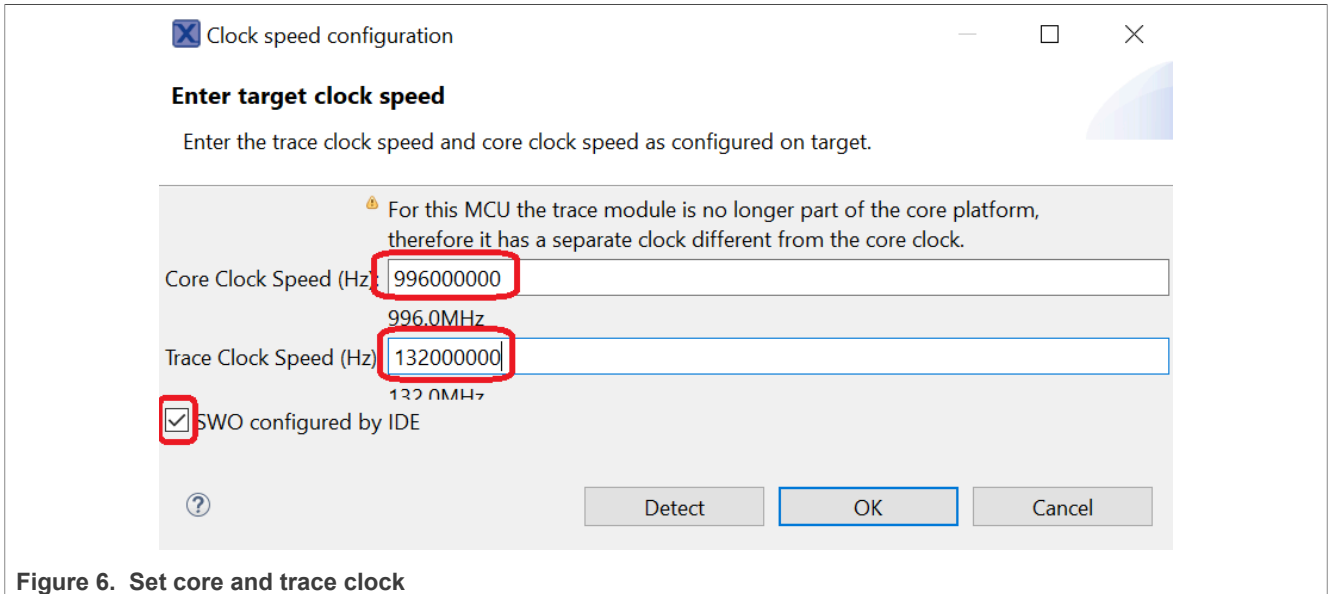


Figure 6. Set core and trace clock

3. Enable the SWO ITM Console and SWO Profile.

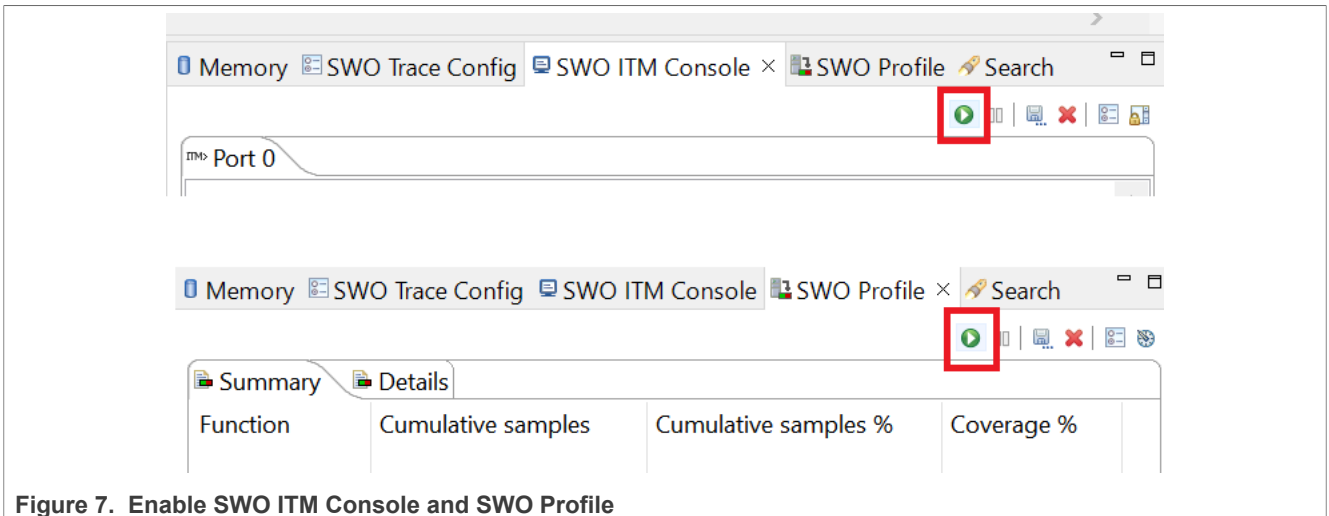


Figure 7. Enable SWO ITM Console and SWO Profile

4. Run

Then we get the SWO profile result, as shown in Figure 8.

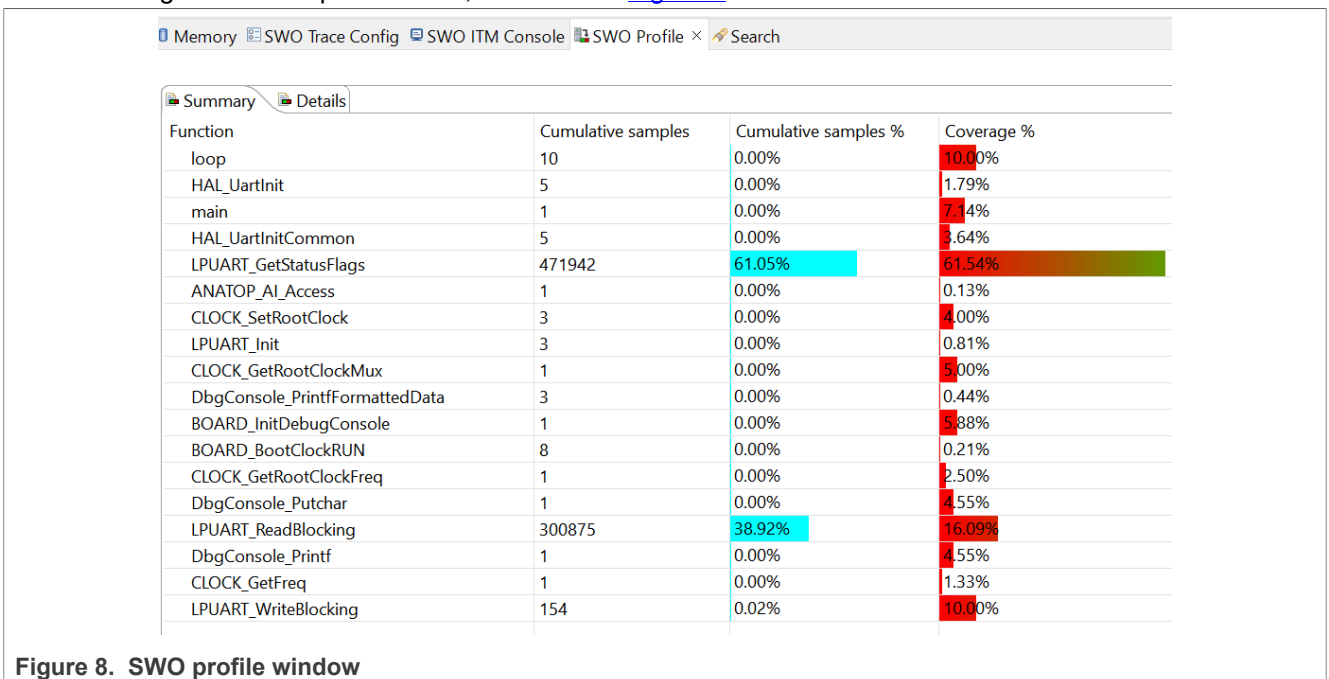


Figure 8. SWO profile window

Type some characters in the UART console on PC, and these characters are also shown in the SWO ITM Console in MCUXpresso.

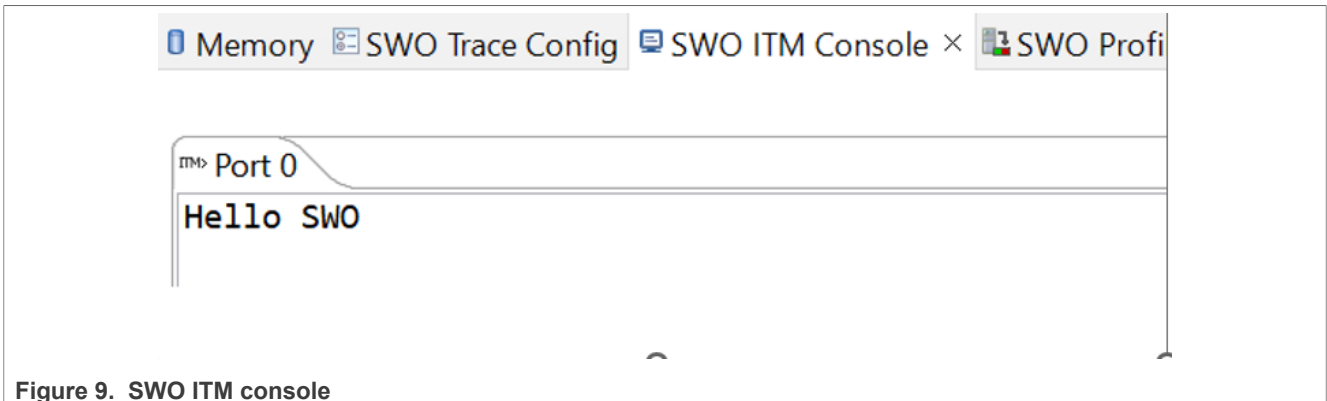


Figure 9. SWO ITM console

Note:

If we do not enable SWO ITM console window, the character is also shown in the **Console** window.

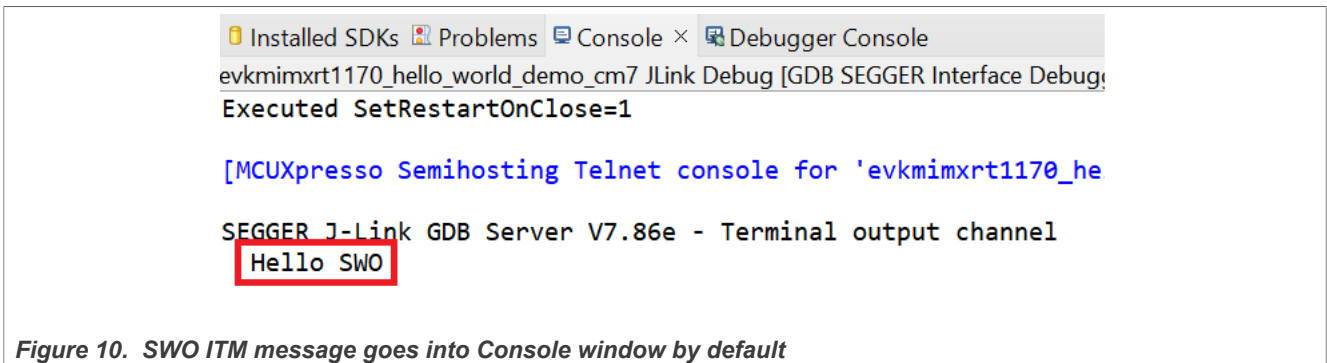


Figure 10. SWO ITM message goes into Console window by default

2.1.3 By IAR

To set up board for LPCLink2-J-Link, see [Section 2.1.1.1](#) first.

The demo project is in AN14701SW.

1. Unzip and open `evkmimxrt1170_swo_demo_cm7_iar` attached in AN14701SW.
2. Configure CPU and SWO clock.

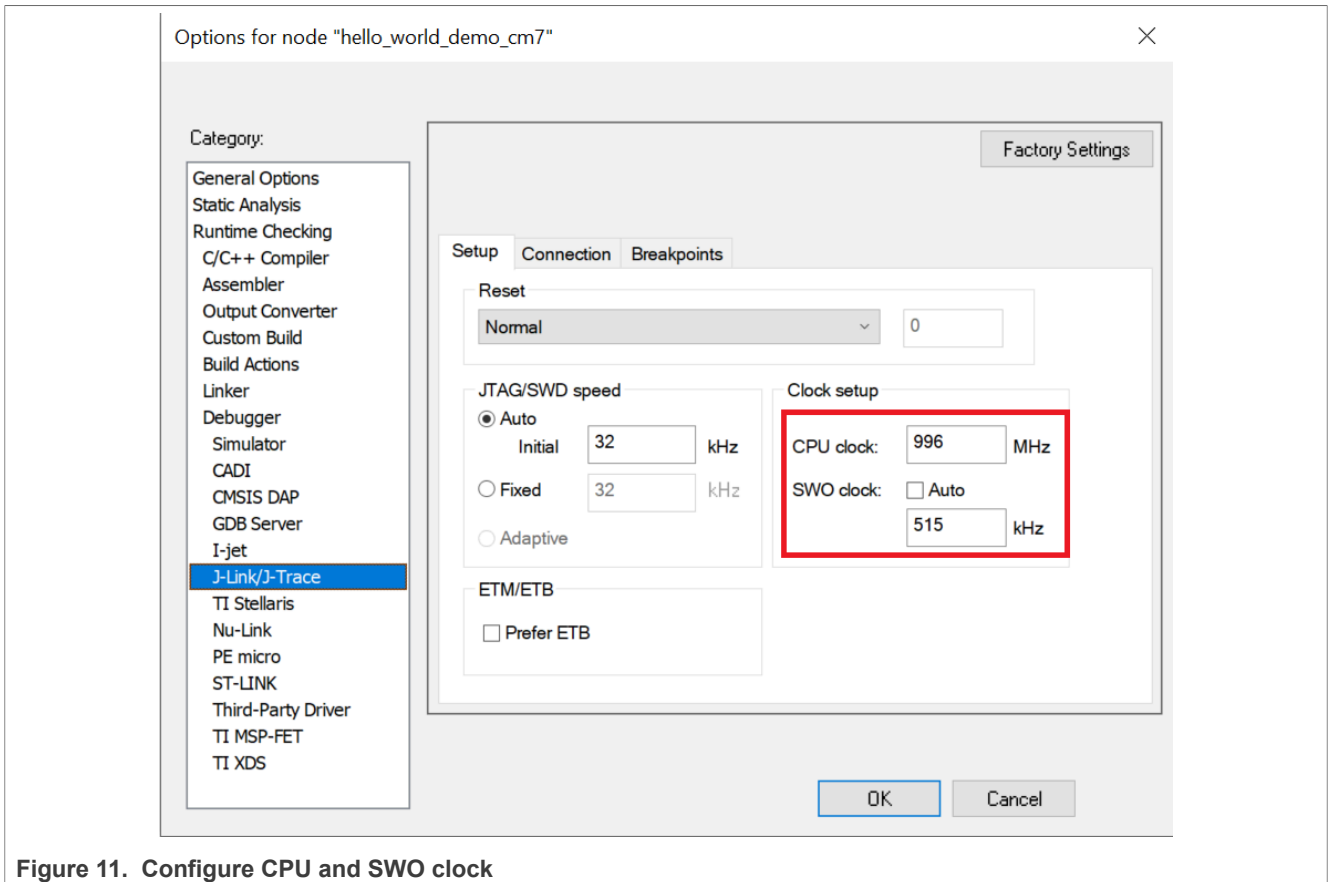


Figure 11. Configure CPU and SWO clock

- Build and run the code, and input some characters from the UART console. The **Function Profiler** window and Terminal I/O window pop up, as shown in [Figure 12](#) and [Figure 13](#).

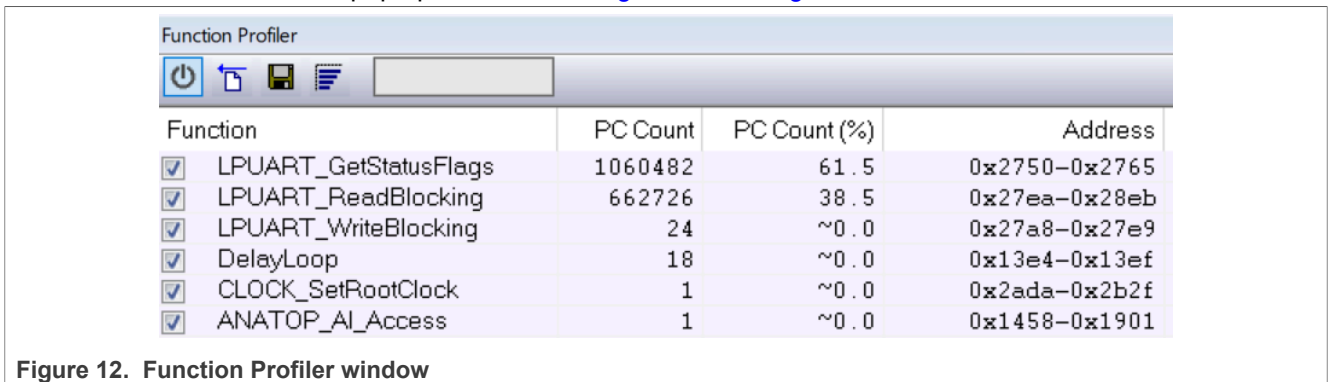


Figure 12. Function Profiler window

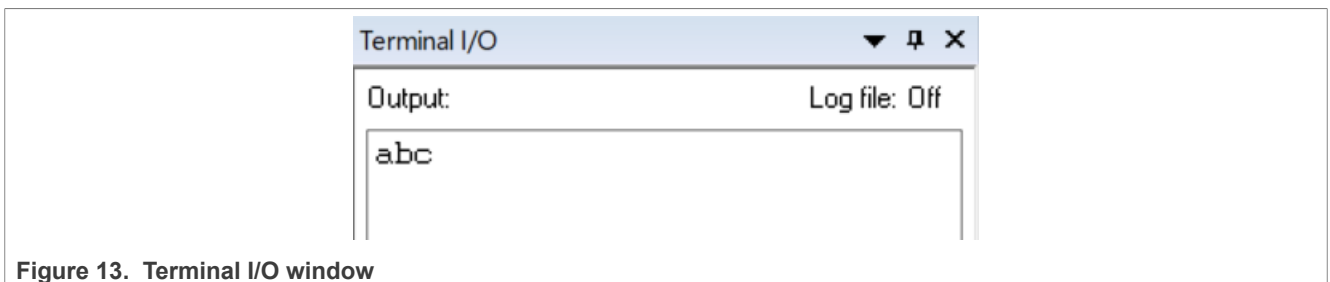


Figure 13. Terminal I/O window

2.1.4 By KEIL

To set up board for LPCLink2-J-Link, see [Section 2.1.1.1](#) first.

The demo project is in AN14071SW.

1. Unzip and open *evkmimxrt1170_swo_demo_cm7_keil* attached in AN14071SW.
2. Configure CPU and SWO clock.

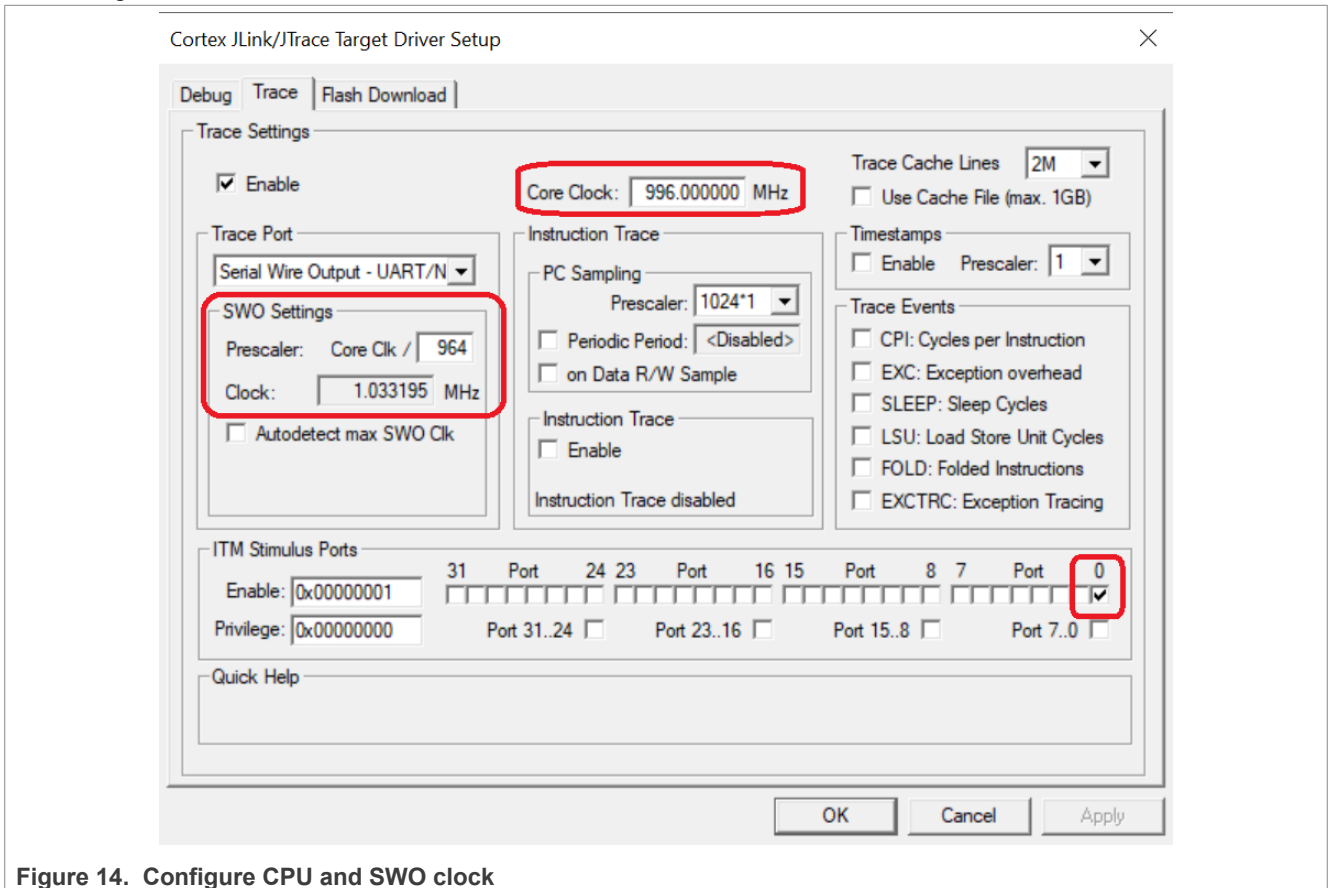


Figure 14. Configure CPU and SWO clock

3. Then build and run the code, input some characters from the UART console, and the **Debug(printf) Viewer** window pops up, as shown in [Figure 15](#).



Figure 15. Debug(printf) Viewer window

4. Halt the core by clicking the  button. The **Instruction Trace** window pops up with the PC sampling result, as shown in [Figure 16](#).

Instruction Trace						
Filter: Execution-All						
Nr.	Ovf	Address	Opcode	INT	Instruction	Source
145	X	0x00004232	9001		STR r0,[sp,#0x04]	
146	X	0x0000466E	9005		STR r0,[sp,#0x14]	
147	X	0x00004234	9801		LDR r0,[sp,#0x04]	873: temp = base->STAT;
148	X	0x0000423A	9801		LDR r0,[sp,#0x04]	875: temp = (base->FIFO &
149	X	0x0000423A	9801		LDR r0,[sp,#0x04]	875: temp = (base->FIFO &
150	X	0x00004656	9809		LDR r0,[sp,#0x24]	
151	X	0x00004230	B082		SUB sp,sp,#0x08	871: {

Figure 16. Instruction Trace window

2.2 SWO trace by J-Link

2.2.1 Board setup for J-Link

Before using the J-Link probe, disconnect J5, J6, J7, J8 (marked in [Figure 1](#)) and then connect J-Link, as shown in [Figure 17](#).



Figure 17. Board setup for J-Link

2.2.2 By MCUXpresso

To set up board for J-Link, perform the steps in [Section 2.1.1.1](#) first.

Most steps are the same as [Section 2.1.2](#).

Differences:

See [Figure 18](#) for SWO configuration.

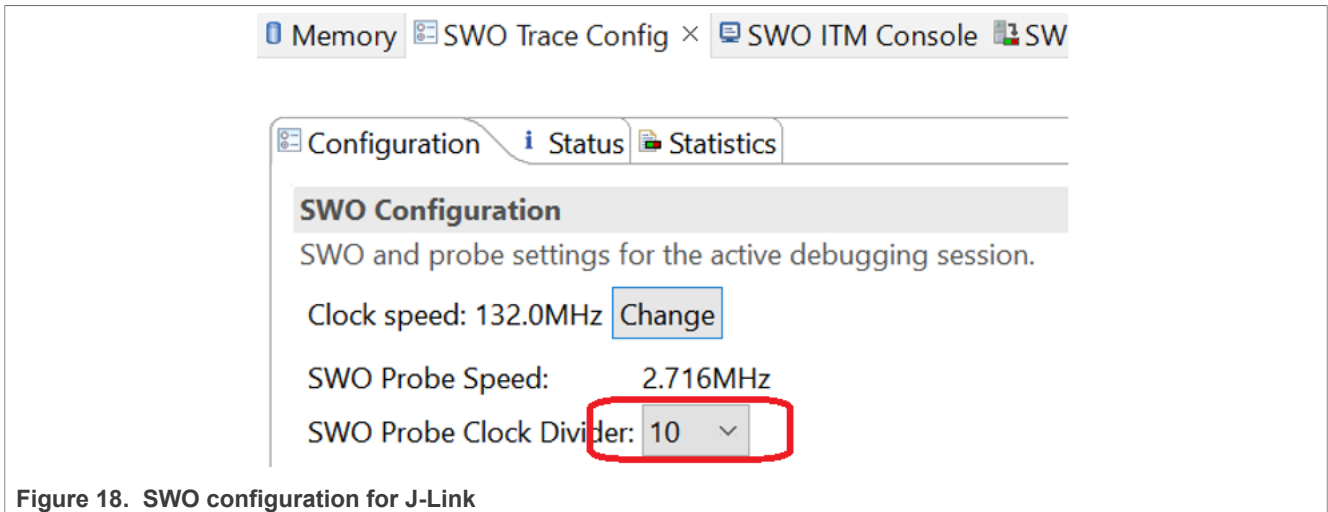


Figure 18. SWO configuration for J-Link

2.2.3 By IAR

For the J-Link probe, see [Section 2.1.3](#) and the steps are the same.

In addition, IAR + J-LINK can work at up to 2.06 MHz. If necessary, to switch the SWO frequency to 2.06 MHz, perform the following steps.

1. Configure the SWO clock in IAR.

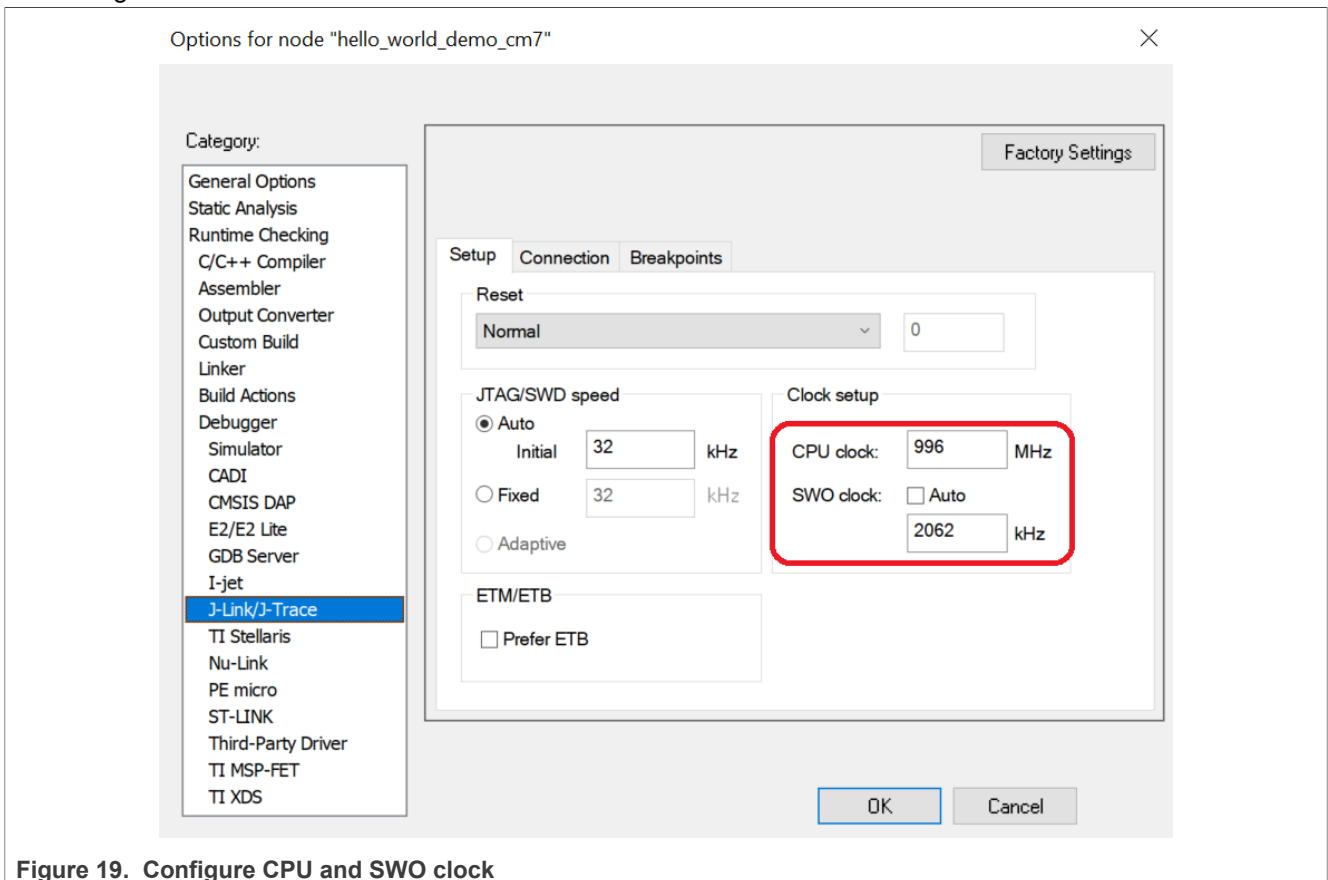


Figure 19. Configure CPU and SWO clock

2. Change the script in `evkmimxrt1170_connect_cm7.mac`, as shown in [Figure 20](#).

```

swo_init()
{
    // funnel
    __writeMemory32(0xC5ACCE55, 0xe0045fb0, "Memory");
    __writeMemory32(0x000003FF, 0xe0045000, "Memory");
    __writeMemory32(0xC5ACCE55, 0xe0043fb0, "Memory");
    __writeMemory32(0x000003FF, 0xe0043000, "Memory");

    __writeMemory32(0xC5ACCE55, 0xe0048fb0, "Memory");
    __writeMemory32(0x00000002, 0xe00480f0, "Memory"); // Select NP7 protocol
    // __writeMemory32(255, 0xe0048010, "Memory"); // 132MHz/256 = 0.515MHz LPCLINK2_JLINK
    writeMemory32(63, 0xe0048010, "Memory"); // 132MHz/64 = 2.062MHz JLINK

    __writeMemory32(0x10009, 0xe000e80, "Memory"); // ITM_TCR = ITM_TCR_BUS_ID | ITM_TCR_ENABLE_L
    __writeMemory32(1, 0xe000e00, "Memory"); // ITM_TER0 = ITM_TER_PORT0;
    __writeMemory32(0x1001, 0xe0001000, "Memory"); // DWT->CTRL = (1U << DWT_CTRL_CYCCNTENA_Pos) ;

    __message "swo_init done";
}
    
```

Figure 20. Configure SWO clock

2.2.4 By KEIL

For J-Link probe, see [Section 2.1.4](#) and the steps are same.

In addition, KEIL + J-LINK can work at up to 26.4 MHz, if necessary, to switch the SWO frequency to 26.4 MHz, perform the following steps.

1. Configure the SWO clock in KEIL.

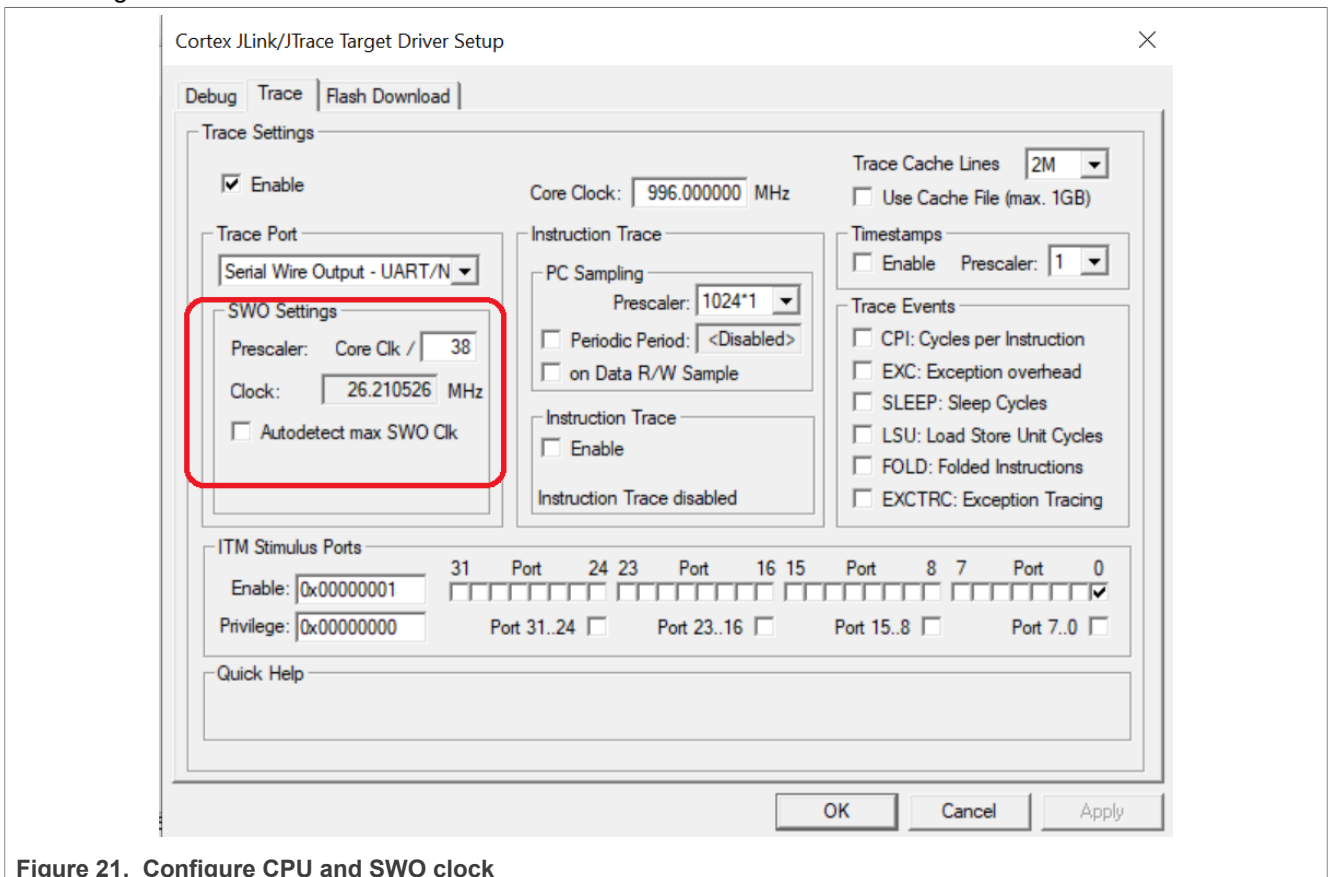


Figure 21. Configure CPU and SWO clock

2. Change the script in `evkmimxrt1170_ram.ini`, as shown in [Figure 22](#).

```

28 FUNC void swo_init(void)
29 {
30     unsigned int value;
31
32     // funnel
33     _WDWORD(0xe0045fb0, 0xc5ACCESS5);
34     _WDWORD(0xe0045000, 0x000003FF);
35     _WDWORD(0xe0043fb0, 0xc5ACCESS5);
36     _WDWORD(0xe0043000, 0x000003FF);
37
38     _WDWORD(0xe0048fb0, 0xc5ACCESS5);
39     _WDWORD(0xe0048000, 0x000003FF); // Select NPT protocol
40     // _WDWORD(0xe0048010, 127); // LPCLINK2_JLINK, 132MHz/128 = 1.033MHz
41     _WDWORD(0xe0048010, 4); // JLINK, 132MHz/5 = 26.4MHz
42
43
44     _WDWORD(0xe0000e80, 0x10009); // ITM_TCR = ITM_TCR_BUS_ID | ITM_TCR_ENABLE_DWT | ITM_TCR_ENABLE_ITM;
45     _WDWORD(0xe0000e00, 1); // ITM_TERO = ITM_TER_PORT0;
46     _WDWORD(0xe0001000, 0x1001); // DWT->CTRL = (1U << DWT_CTRL_CYCCNTENA_Pos) | (1U << DWT_CTRL_PCSAMPLENA_Pos);
47 }
    
```

Figure 22. Configure SWO clock

Note: In this condition, as there is a lot of transactions for PC sampling, the character sent to Debug(printf) viewer is less than we actually sent. To solve this issue, comment line 46 in evkmimxrt1170_ram.ini to disable PC sampling.

2.3 SWO trace by μTRACE

2.3.1 Board setup for μTrace

For board setup, refer to [Figure 23](#). Disconnect J5, J6, J7, J8 (marked in [Figure 1](#)), and connect the μTrace cable.

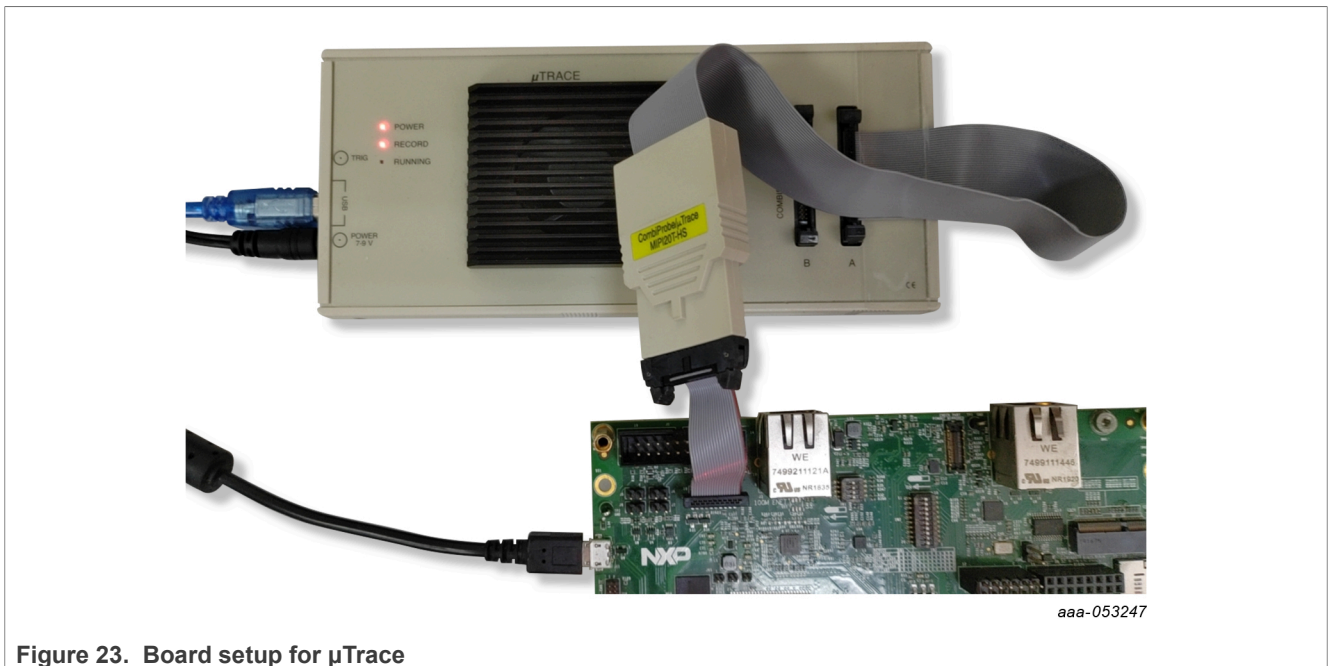


Figure 23. Board setup for μTrace

2.3.2 By TRACE32

2.3.2.1 SWO trace for ITM console

To perform SWO trace for the ITM console, perform the following steps:

1. Unzip evkmimxrt1170_swo_demo_cm7_trace32.7z to directory - C:\T32\demo\arm\hardware\imxrt\imxrt117x\imxrt1170-evk\evkmimxrt1170_hello_world_demo_cm7_swo_utrace.

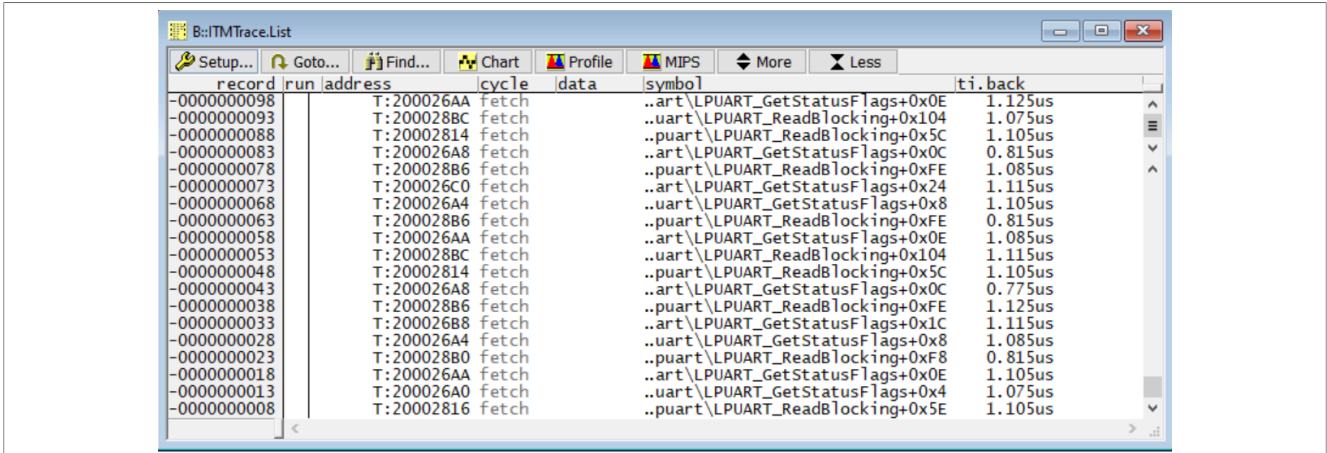


Figure 26. PC samples

2.4 ETM trace by J-Trace

2.4.1 Hardware setup for J-Trace

1. Sold R1881-1885.

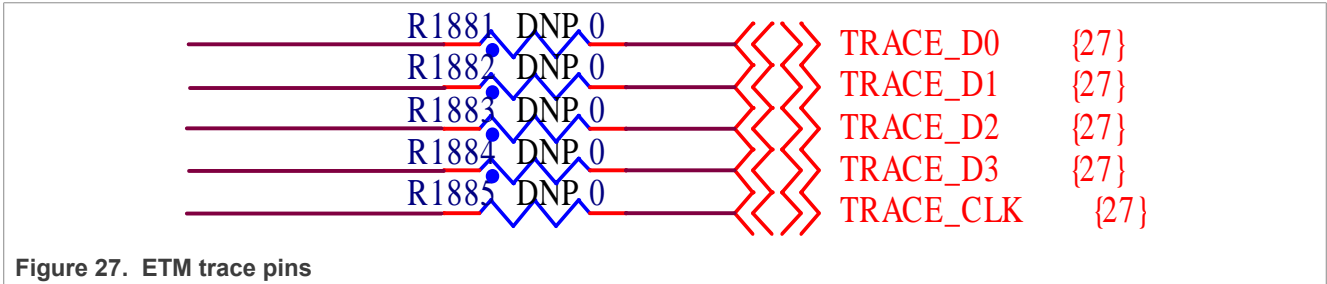


Figure 27. ETM trace pins

For R1881-1885 place on board, refer to [Figure 28](#) and [Figure 29](#).

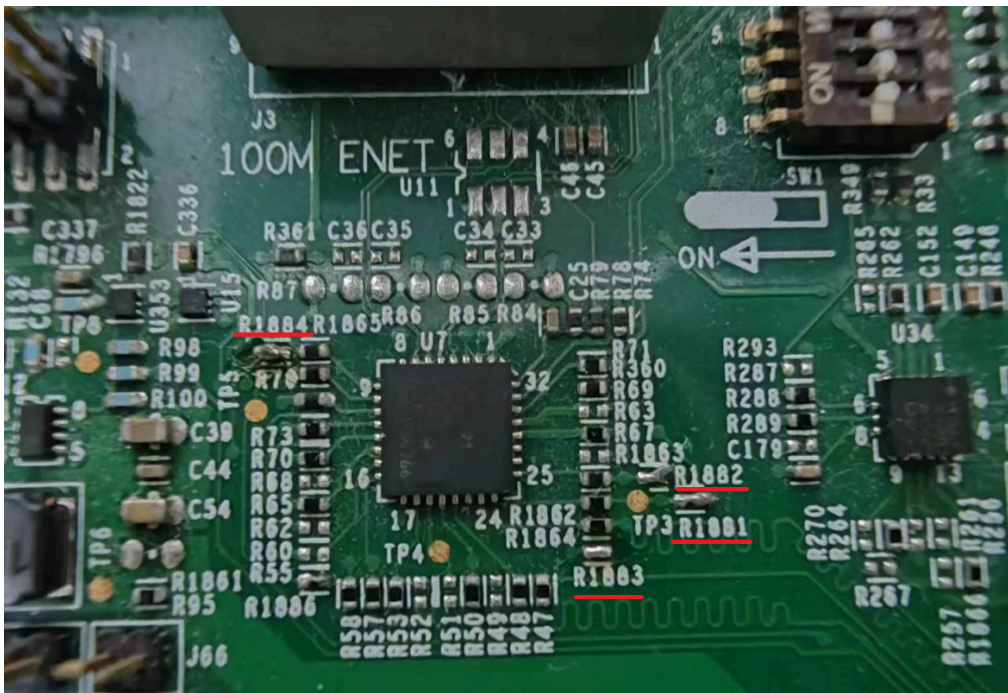


Figure 28. Place for R1881 – 1884 (On the top side)

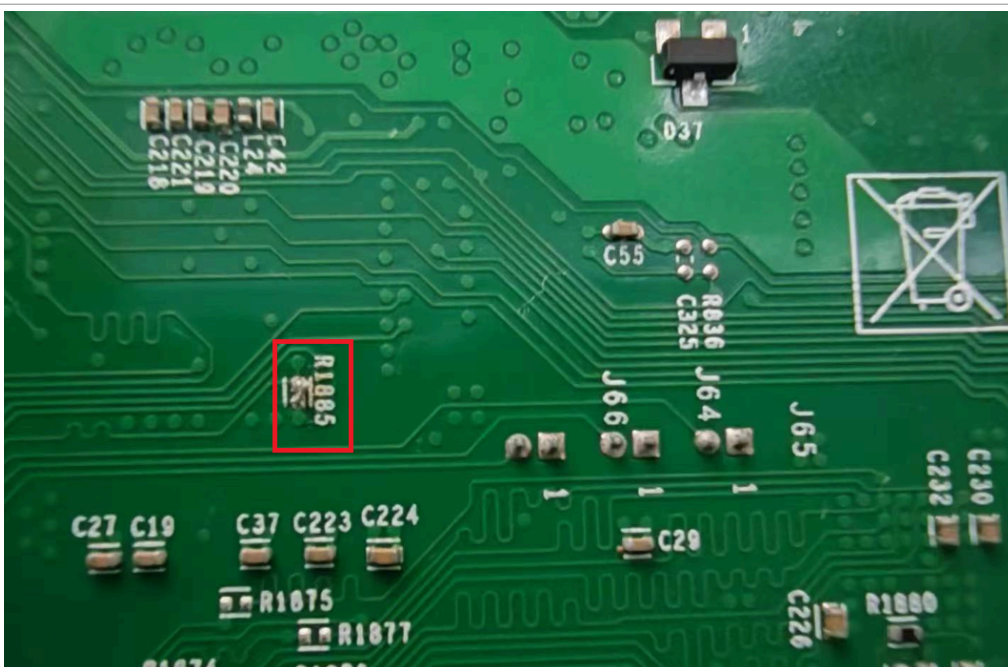
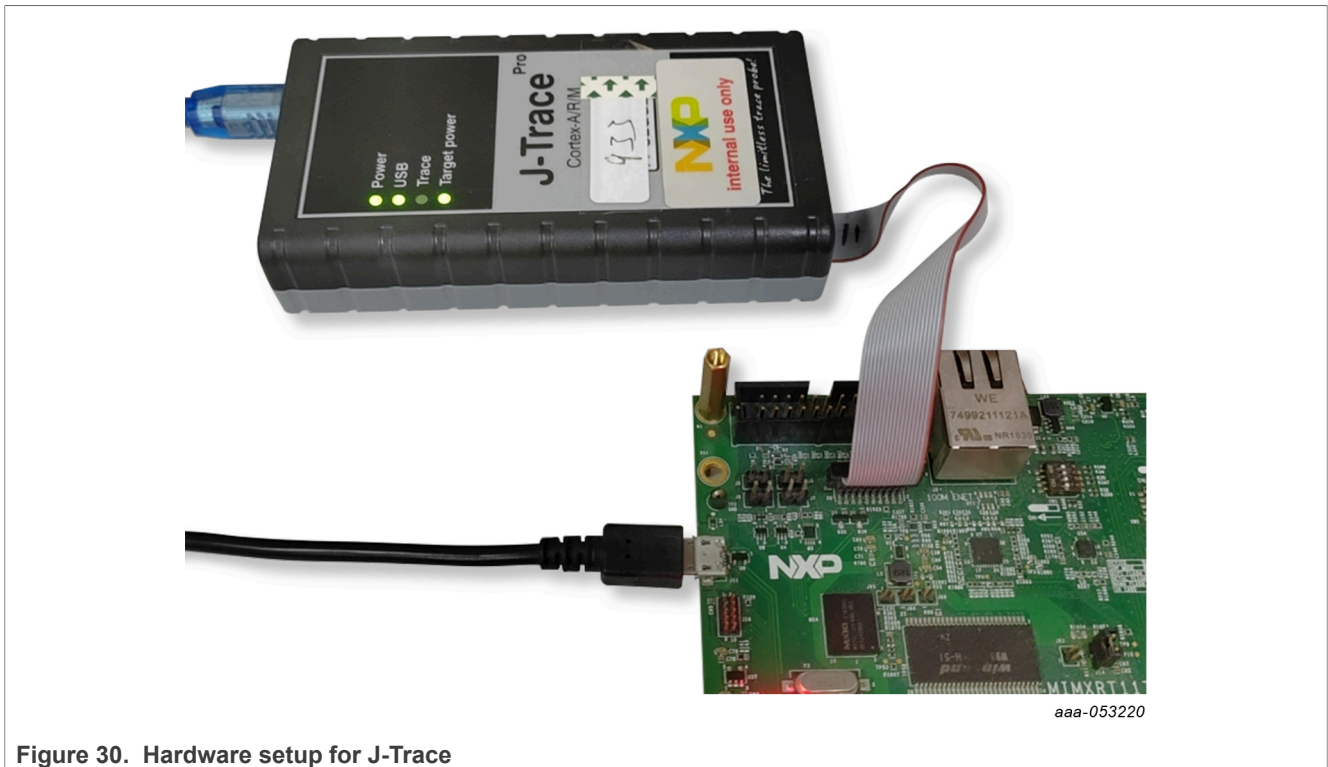


Figure 29. Place for R1885 (On the bottom side)

2. Disconnect J5, J6, J7, and J8 (marked in [Figure 1](#)).
3. Connect the J-Trace cable, as shown in [Figure 30](#).




aaa-053220

Figure 30. Hardware setup for J-Trace

2.4.2 By Ozone

Perform the following steps:

1. Download the example code [NXP_iMXRT1176_M7_TracePins.zip](#) provided by Segger.
2. Unzip this code.
3. Open Ozone, execute **File** → **Open**, and select **NXP_iMRT1176_M7_TracePins\Ozone.jdebug** from the folder unzipped in [Step 2](#).
4. Press the download and reset button , and then go into the ETM trace state.

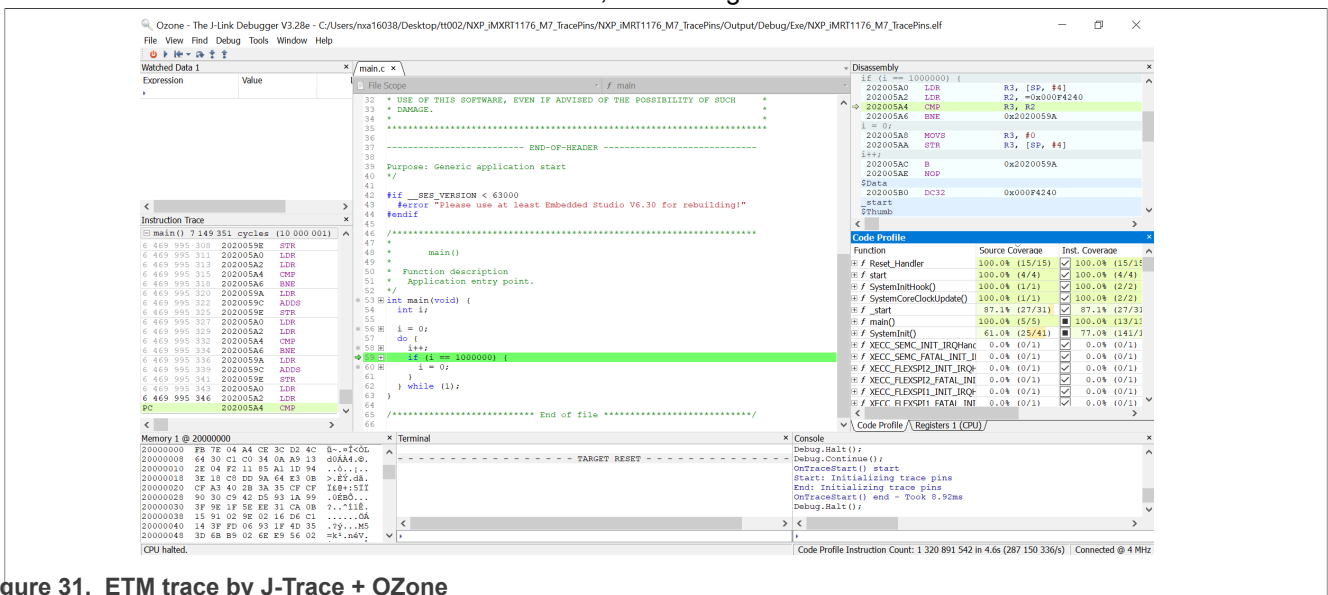


Figure 31. ETM trace by J-Trace + Ozone

2.5 ETM trace by μ TRACE

About ETM trace by μ TRACE on i.MX RT1170, see *How to Enable Embedded Trace Macrocell (ETM) Trace for i.MXRT11xx Series* (document [AN14046](#)).

2.6 Implement trace on i.MX RT1170 EVKB

On the i.MX RT1170 EVKB, as `JTAG_nTRST` is driven low by default, it blocks the trace feature. To avoid this issue, one workaround is to set `GPIO_LPSR_10` to **GPIO** instead of **JTAG_nTRST**.

- Reference script for J-Link/J-Trace: `Target.WriteU32(0x40c08028, 0xa)`
- Reference script for uTrace: `Data.Set AD:0x40c08028 %Long 0x0000000a`

3 Reference

1. [ARMv7-M Architecture Reference Manual](#)

4 Note about the source code in the document

Example code shown in this document has the following copyright and BSD-3-Clause license:

Copyright 2023 NXP Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met:

1. Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer.
2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution.
3. Neither the name of the copyright holder nor the names of its contributors may be used to endorse or promote products derived from this software without specific prior written permission.

THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS "AS IS" AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE COPYRIGHT HOLDER OR CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

5 Revision history

[Table 2](#) summarizes the revisions to this document.

Table 2. Revision history

Revision number	Release date	Description
1	13 November 2023	Initial public release

Legal information

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <https://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, μ Vision, Versatile — are trademarks and/or registered trademarks of Arm Limited (or its subsidiaries or affiliates) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved.

IAR — is a trademark of IAR Systems AB.

i.MX — is a trademark of NXP B.V.

J-Link — is a trademark of SEGGER Microcontroller GmbH.

Microsoft, Azure, and ThreadX — are trademarks of the Microsoft group of companies.

Contents

1	Introduction	2
2	Implementation	2
2.1	SWO trace by onboard LPCLink2 J-Link	2
2.1.1	Board setup for LPCLink2 J-Link	2
2.1.1.1	Enable LPCLINK2 J-Link on i.MX RT1170 EVK	2
2.1.1.2	Jumper settings	4
2.1.2	By MCUXpresso	5
2.1.3	By IAR	7
2.1.4	By KEIL	9
2.2	SWO trace by J-Link	10
2.2.1	Board setup for J-Link	10
2.2.2	By MCUXpresso	10
2.2.3	By IAR	11
2.2.4	By KEIL	12
2.3	SWO trace by μ TRACE	13
2.3.1	Board setup for μ Trace	13
2.3.2	By TRACE32	13
2.3.2.1	SWO trace for ITM console	13
2.3.2.2	SWO trace for PC sampling	14
2.4	ETM trace by J-Trace	15
2.4.1	Hardware setup for J-Trace	15
2.4.2	By Ozone	17
2.5	ETM trace by μ TRACE	18
2.6	Implement trace on i.MX RT1170 EVKB	18
3	Reference	18
4	Note about the source code in the document	18
5	Revision history	18
	Legal information	19

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.