AN14251

i.MX RT1xxx – Ethernet Capabilities and PHY Connection

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Document information

Information	Content
Keywords	NETC, ENET, i.MX RT1xxx, PHY, Ethernet
Abstract	This document describes i.MX RT1xxx MCUs Ethernet capabilities and options for PHY connection.

1 Introduction

This document describes i.MX RT1xxx MCUs Ethernet capabilities and options for the PHY (ISO/OSI physical layer) connection. Because the PHY is not integrated in the MCU, an external PHY must be used to connect the MCU into the Ethernet network. For the PHY connection, a Media-independent interface is used. i.MX RT1xxx supports three variants of the interface: Media-Independent Interface (MII), Reduced Media-Independent Interface (RMII), and devices with Gigabit Ethernet. It also supports Reduced Gigabit Media-Independent Interface (RGMII).

2 Media-independent interface

The media-independent interface was originally defined to connect the Media Access Control (MAC) block to the PHY chip. Being media-independent means that different types of PHY devices for connecting to different media (for example, twisted pair, fiber optic) can be used without redesigning or replacing the MAC hardware. The original MII design has been extended to support reduced signals and increased speeds. The current variants include:

- Reduced Media-Independent Interface (RMII)
- Gigabit Media-Independent Interface (GMII)
- Reduced Gigabit Media-Independent Interface (RGMII)
- Serial Media-Independent Interface (SMII)
- Serial Gigabit Media-Independent Interface (SGMII)
- High Serial Gigabit Media-Independent Interface (HSGMII)
- Quad Serial Gigabit Media-Independent Interface (QSGMII)
- 10-gigabit Media-Independent Interface (XGMII)

2.1 Media-independent interface signals

As it is mentioned in the introduction, MCUs from the i.MX RT family support MII, RMII, and RGMII interface variants. In the tables below, there is a summary of required and optional signals for each variant.

2.1.1 MII signals

Table 1. MII transmit signals

Signal name	Description	Direction
TX_CLK	Transmit clock	PHY to MAC
TXD[0..3]	Transmit data bit 0 - 3	MAC to PHY
TX_EN	Transmit enable	MAC to PHY
TX_ER	Transmit error (optional)	MAC to PHY

Table 2. MII receive signals

Signal name	Description	Direction
RX_CLK	Receive clock	PHY to MAC
RXD[0..3]	Receive data bit 0 - 3	PHY to MAC
RX_DV	Receive data valid	PHY to MAC
RX_ER	Receive error	PHY to MAC

Table 2. MII receive signals*...continued*

Signal name	Description	Direction
CRS	Carrier sense	PHY to MAC
COL	Collision detect	PHY to MAC

2.1.2 RMII signals

Table 3. RMII transmit signals

Signal name	Description	Direction
REF_CLK	Continuous 50 MHz reference clock	MAC to PHY or PHY to MAC
TXD0	Transmit data bit 0	MAC to PHY
TXD1	Transmit data bit 1	MAC to PHY
TX_EN	When high, clock data on TXD0 and TXD1 to the transmitter	MAC to PHY

Table 4. RMII receive signals

Signal name	Description	Direction
RXD0	Receive data bit 0	PHY to MAC
RXD1	Receive data bit 1	PHY to MAC
CRS_DV	Carrier Sense (CRS) and RX Data Valid (RX_DV) multiplexed on alternate clock cycles. In 10 Mbit/s mode, it alternates every 10 clock cycles.	PHY to MAC
RX_ER	Receive error (optional on switches)	PHY to MAC

2.1.3 RGMII signals

Table 5. RGMII transmit signals

Signal name	Description	Direction
TXC	Transmit clock signal	MAC to PHY
TXD[0..3]	Transmit data bit 0 - 3	MAC to PHY
TX_CTL	Multiplexing of transmitter enabled and transmitter error	MAC to PHY

Table 6. RGMII receive signals

Signal name	Description	Direction
RXC	Received clock signal (recovered from the incoming received data)	PHY to MAC
RXD[0..3]	Receive data bit 0 - 3	PHY to MAC
RX_CTL	Multiplexing of data received is valid and receiver error	PHY to MAC

3 Ethernet capabilities

Ethernet is an integral part of all consumer, industrial and automotive applications. This is the reason why all i.MX RT1xxx devices contain at least one Ethernet module that allows connecting the device to the Ethernet network. Table 7 summarizes all i.MX RT1xxx devices and their Ethernet capabilities.

Table 7. i.MX RT1xxx Ethernet capabilities

Device	Fast Ethernet (10/100 Mbps)	Gigabit Ethernet (10/100/1000 Mbps)	Ethernet switch (10/100/1000 Mbps)
i.MX RT101x	-	-	-
i.MX RT102x	1x	-	-
i.MX RT105x	1x	-	-
i.MX RT106x	1x	-	-
i.MX RT117x	1x	1x (AVB support) 1x (AVB + TSN support)	
i.MX RT118x	-	2x (TSN support)	1x (5 port, TSN support)

4 MCU PHY connection

As it was mentioned before, each i.MX RT1xxx device except i.MX RT101x supports at least one Ethernet interface that requires an external PHY to be able to communicate in the Ethernet network. Devices that have Fast Ethernet interface support Media-Independent Interface (MII) and Reduced Media-Independent Interface (RMII). Devices with Gigabit Ethernet also support Reduced Gigabit Media-Independent Interface (RGMII). All Ethernet capable devices support Serial Management Interface (SMI). This interface is implemented by two signals, MDIO (bidirectional data signal) and MDC (clock-driven by the MAC device to the PHY) and it is used to read and write the control and status registers of the PHY to configure each PHY before operation.

4.1 i.MX RT102x

The i.MX RT102x family provides one Fast Ethernet interface that supports the MII and RMII connection between the MAC and the PHY.

4.1.1 MII, RMII, and MDIO available pins

Table 8, Table 9, and Table 10 list all the available pins that can be used to connect the PHY via MII and RMII.

Table 8. i.MX RT102x – MII pads

ENET		MII		
General signal name	MCU signal name	MCU port name	MCU pad	Dir
TX_CLK	TX_CLK	ENET_TX_CLK	GPIO_SD_B1_04 GPIO_AD_B0_08	I
TXD0	TX_DATA0	ENET_TX_DATA0	GPIO_SD_B1_10 GPIO_AD_B0_14	O
TXD1	TX_DATA1	ENET_TX_DATA1	GPIO_SD_B1_11 GPIO_AD_B0_15	O
TXD2	TX_DATA2	ENET_TX_DATA2	GPIO_EMC_41	O
TXD3	TX_DATA3	ENET_TX_DATA3	GPIO_EMC_40	O

Table 8. i.MX RT102x – MII pads*...continued*

ENET		MII		
General signal name	**MCU signal name**	**MCU port name**	**MCU pad**	**Dir**
TX_EN	TX_EN	ENET_TX_EN	GPIO_SD_B1_09 GPIO_AD_B0_13	O
TX_ER (optional)	TX_ER	ENET_TX_ER	GPIO_EMC_39	O
RX_CLK	RX_CLK	ENET_RX_CLK	GPIO_EMC_36	I
RXD0	RX_DATA0	ENET_RX_DATA0	GPIO_SD_B1_06 GPIO_AD_B0_10	I
RXD1	RX_DATA1	ENET_RX_DATA1	GPIO_SD_B1_05 GPIO_AD_B0_09	I
RXD2	RX_DATA2	ENET_RX_DATA2	GPIO_EMC_38	I
RXD3	RX_DATA3	ENET_RX_DATA3	GPIO_EMC_37	I
RX_DV	RX_EN	ENET_RX_EN	GPIO_SD_B1_07 GPIO_AD_B0_11	I
RX_ER	RX_ER	ENET_RX_ER	GPIO_SD_B1_08 GPIO_AD_B0_12	I
CRS	CRS	ENET_CRS	GPIO_EMC_34	I
COL	COL	ENET_COL	GPIO_EMC_35	I

Table 9. i.MX RT102x – RMII pads

ENET		RMII		
General signal name	**MCU signal name**	**MCU port name**	**MCU pin**	**Dir**
REF_CLK	REF_CLK1	ENET_REF_CLK	GPIO_SD_B1_04 GPIO_AD_B0_08	I/O
TXD0	TX_DATA0	ENET_TX_DATA0	GPIO_SD_B1_10 GPIO_AD_B0_14	O
TXD1	TX_DATA1	ENET_TX_DATA1	GPIO_SD_B1_11 GPIO_AD_B0_15	O
TX_EN	TX_EN	ENET_TX_EN	GPIO_SD_B1_09 GPIO_AD_B0_13	O
RXD0	RX_DATA0	ENET_RX_DATA0	GPIO_SD_B1_06 GPIO_AD_B0_10	I
RXD1	RX_DATA1	ENET_RX_DATA1	GPIO_SD_B1_05 GPIO_AD_B0_09	I
CRS_DV	RX_EN	ENET_RX_EN	GPIO_SD_B1_07 GPIO_AD_B0_11	I
RX_ER	RX_ER	ENET_RX_ER	GPIO_SD_B1_08 GPIO_AD_B0_12	I

Table 10. i.MX RT102x – MDIO pads

ENET		MDIO		
General signal name	MCU signal name	MCU port name	MCU pin	Dir
MDC	MDC	ENET_MDC	GPIO_EMC_41 GPIO_SD_B0_03 GPIO_AD_B0_05	O
MDIO	MDIO	ENET_MDIO	GPIO_EMC_40 GPIO_SD_B0_02 GPIO_AD_B0_04	I/O

4.1.2 MII / RMII pin and clock configuration

According to the required connection (MII/RMII), select and configure one of the pins for each signal listed in Table 8 (MII) or Table 9 (RMII). Do the same with the MDC and MDIO signals listed in Table 10.

The pin functionality is configured via the `SW_MUX_CTL_PAD_GPIO_n_SW MUX` control register. The pin direction is automatically determined by the selected functionality and it is listed in the column Dir.

Use the settings below for each selected pin and write the settings into the `SW_PAD_CTL_PAD_GPIO_n SW PAD` control register.

- Hysteresis – disabled
- Open Drain – disabled
- Speed - 150 MHz - 200 MHz
- Drive Strength - R 0/5
- Slew Rate - Fast Slew Rate

Output pins (see the Dir column in the tables above):

- Pull Up / Down Config - 100 K ohm Pull Down (does not have effect)
- Pull / Keep Select – Keeper (does not have effect)
- Pull / Keep Enable - Pull/Keeper Disabled

Input pins (see the Dir column in the tables above):

- Pull Up / Down Config - 100 K ohm Pull Down
- Pull / Keep Select – Pull
- Pull / Keep Enable - Pull/Keeper Enabled

MDIO signal:

- Use the settings for input pins.

4.1.2.1 MII connection-specific settings

- Set the `ENET_TX_CLK_SEL` bit to 1 in `IOMUXC_GPR_GPR1`.
- The `ipg_clock_root` frequency must be 25 MHz or higher.

4.1.2.2 RMII connection-specific settings

When the RMII connection is used, there are 2 possible ways to generate an RMII reference clock.

1. The RMII reference clock is provided by the MCU (the `ENET_REF_CLK` port is output). The following configurations must be used.
2. The RMII reference clock is provided by the 50 MHz external oscillator (the `ENET_REF_CLK` port is input).

The reference clock is provided by the MCU:

- Set the Sion bit in the SW_MUX_CTL_PAD_GPIO_n_SW MUX control register for the ENET_REF_CLK pin to 1.
- Use the settings for output pins for ENET_REF_CLK in the SW_PAD_CTL_PAD_GPIO_n SW PAD control register.
- Enable the ENET_PLL 500 MHz output and set DIV_SELECT to 1. This is configured via the CCM_ANALOG_PLL_ENETn register. For the correct PLL initialization, read an appropriate chapter in the reference manual.
- Set the ENET_REF_CLK_DIR bit in the IOMUXC_GPR_GPR1 register to 1 (ENET_REF_CLK is output-driven by ENET_PLL).
- The ipg_clock_root frequency must be 50 MHz or higher.

The reference clock is provided by the 50 MHz external oscillator:

- Use the settings for input pins for ENET_REF_CLK in the SW_PAD_CTL_PAD_GPIO_n SW PAD control register.
- Set the ENET_REF_CLK_DIR bit in the IOMUXC_GPR_GPR1 register to 0 (ENET_REF_CLK is input).
- The ipg_clock_root frequency must be 50 MHz or higher.
- The ipg_clock_root frequency must be 50 MHz or higher.

4.2 i.MX RT105x

The i.MX RT105x family provides one Fast Ethernet interface that supports the MII and RMII connection between the MAC and the PHY.

4.2.1 MII, RMII, and MDIO available pins

Table 11. i.MX RT105x – MII pads

ENET		MII		
General signal name	**MCU signal name**	**MCU port name**	**MCU pin**	**Dir**
TX_CLK	ENET_TX_CLK	ENET_TX_CLK	GPIO_EMC_25 GPIO_B1_10	I
TXD0	ENET_TX_DATA0	ENET_TX_DATA0	GPIO_EMC_22 GPIO_B1_07	O
TXD1	ENET_TX_DATA1	ENET_TX_DATA1	GPIO_EMC_21 GPIO_B1_08	O
TXD2	ENET_TX_DATA2	ENET_TX_DATA2	GPIO_AD_B0_05	O
TXD3	ENET_TX_DATA3	ENET_TX_DATA3	GPIO_AD_B0_04	O
TX_EN	ENET_TX_EN	ENET_TX_EN	GPIO_EMC_24 GPIO_B1_09	O
TX_ER (optional)	ENET_TX_ER	ENET_TX_ER	GPIO_AD_B0_07	O
RX_CLK	ENET_RX_CLK	ENET_RX_CLK	GPIO_AD_B0_06	I
RXD0	ENET_RX_DATA0	ENET_RX_DATA0	GPIO_EMC_20 GPIO_B1_04	I
RXD1	ENET_RX_DATA1	ENET_RX_DATA1	GPIO_EMC_19 GPIO_B1_05	I
RXD2	ENET_RX_DATA2	ENET_RX_DATA2	GPIO_AD_B0_09	I
RXD3	ENET_RX_DATA3	ENET_RX_DATA3	GPIO_AD_B0_08	I

Table 11. i.MX RT105x – MII pads*...continued*

ENET		MII		
General signal name	**MCU signal name**	**MCU port name**	**MCU pin**	**Dir**
RX_DV	ENET_RX_EN	ENET_RX_EN	GPIO_EMC_23 GPIO_B1_06	I
RX_ER	ENET_RX_ER	ENET_RX_ER	GPIO_EMC_26 GPIO_B1_11	I
CRS	ENET_CRS	ENET_CRS	GPIO_AD_B0_10	I
COL	ENET_COL	ENET_COL	GPIO_AD_B0_11	I

Table 12. i.MX RT105x – RMII pads

ENET		RMII		
General signal name	**MCU signal name**	**MCU port name**	**MCU pin**	**Dir**
REF_CLK	ENET_REF_CLK	ENET_REF_CLK	GPIO_EMC_25 GPIO_B1_10	I/O
TXD0	ENET_TX_DATA0	ENET_TX_DATA0	GPIO_EMC_22 GPIO_B1_07	O
TXD1	ENET_TX_DATA1	ENET_TX_DATA1	GPIO_EMC_21 GPIO_B1_08	O
TX_EN	ENET_TX_EN	ENET_TX_EN	GPIO_EMC_24 GPIO_B1_09	O
RXD0	ENET_RX_DATA0	ENET_RX_DATA0	GPIO_EMC_20 GPIO_B1_04	I
RXD1	ENET_RX_DATA1	ENET_RX_DATA1	GPIO_EMC_19 GPIO_B1_05	I
CRS_DV	ENET_RX_EN	ENET_RX_EN	GPIO_EMC_23 GPIO_B1_06	I
RX_ER	ENET_RX_ER	ENET_RX_ER	GPIO_EMC_26 GPIO_B1_11	I

Table 13. i.MX RT105x – MDIO pads

ENET		MDIO		
General signal name	**MCU signal name**	**MCU port**	**MCU pin**	**Dir**
MDC	ENET_MDC	ENET_MDC	GPIO_EMC_40 GPIO_B1_14 GPIO_AD_B1_04	O
MDIO	ENET_MDIO	ENET_MDIO	GPIO_EMC_41 GPIO_B1_15 GPIO_AD_B1_05	I/O

4.2.2 MII/RMII pin and clock configuration

According to the required connection (MII/RMII), select and configure one of the pins for each signal listed in Table 11 (MII) or Table 12 (RMII). Do the same with the MDC and MDIO signals listed in Table 13.

The pin functionality is configured via the SW_MUX_CTL_PAD_GPIO_n_SW MUX control register. The pin direction is automatically determined by the selected functionality and it is listed in the column Dir.

Use the settings below for each selected pin and write the settings into the SW_PAD_CTL_PAD_GPIO_n SW PAD control register.

- Hysteresis – disabled
- Open Drain – disabled
- Speed - 150 MHz - 200 MHz
- Drive Strength - R0/5
- Slew Rate - Fast Slew Rate

Output pins (see the Dir column in the tables above):

- Pull Up / Down Config - 100 K ohm Pull Down (does not have effect)
- Pull / Keep Select – Keeper (does not have effect)
- Pull / Keep Enable - Pull/Keeper Disabled

Input pins (see the Dir column in the tables above):

- Pull Up / Down Config - 100 K ohm Pull Down
- Pull / Keep Select – Pull
- Pull / Keep Enable - Pull/Keeper Enabled

MDIO signal:

- Use settings for input pins

4.2.2.1 MII connection-specific settings

- Set the ENET_TX_CLK_SEL bit to 1 in the IOMUXC_GPR_GPR1 register.
- The ipg_clock_root frequency must be 25 MHz or higher.

4.2.2.2 RMII connection-specific settings

When the RMII connection is used, there are 2 possible ways to generate an RMII reference clock.

1. The RMII reference clock is provided by the MCU (ENET_REF_CLK is output). The following configuration must be used.
2. The RMII reference clock is provided by the 50 MHz external oscillator (the ENET_REF_CLK port is input).

The reference clock is provided by the MCU:

- Set the Sion bit in the SW_MUX_CTL_PAD_GPIO_n_SW MUX control register for the ENET_REF_CLK pin to 1.
- Use the settings for output pins for ENET_REF_CLK in the SW_PAD_CTL_PAD_GPIO_n SW PAD control register.
- Enable the ENET_PLL output and set DIV_SELECT to 1. This is configured via the CCM_ANALOG_PLL_ENETn register. For the correct PLL initialization, read an appropriate chapter in the reference manual.
- Set the ENET_REF_CLK_DIR bit in the IOMUXC_GPR_GPR1 register to 1 (ENET_REF_CLK is output-driven by ENET_PLL).
- The ipg_clock_root frequency must be 50 MHz or higher.

The reference clock is provided by the 50 MHz external oscillator:

- Use the settings for input pins for ENET_REF_CLK in the SW_PAD_CTL_PAD_GPIO_n SW PAD control register.
- Set the ENET_REF_CLK_DIR bit in the IOMUXC_GPR_GPR1 register to 0 (ENET_REF_CLK is input).
- The ipg_clock_root frequency must be 50 MHz or higher.
- The ipg_clock_root frequency must be 50 MHz or higher.

4.3 i.MX RT106x

The i.MX RT106x family provides two Fast Ethernet interfaces, ENET and ENET2 that support the MII and RMII connection between the MAC and the PHY. Both interfaces can be used at the same time independently regardless of the MII or RMII mode configured. Each interface has to use a different set of pins. MDIO, MDC pins can be shared by more PHYs or each PHY can be connected to an individual pair of MDC, MDIO pins.

4.3.1 ENET MII, RMII, and MDIO available pins

Table 14. i.MX RT106x – ENET MII pads

ENET		MII		
General signal name	**MCU signal name**	**MCU port**	**MCU pin**	**Dir**
TX_CLK	TX_CLK	ENET_TX_CLK	GPIO_EMC_25 GPIO_B1_10	I
TXD0	TDATA0	ENET_TX_DATA0	GPIO_EMC_22 GPIO_B1_07	O
TXD1	TDATA1	ENET_TX_DATA1	GPIO_EMC_21 GPIO_B1_08	O
TXD2	TDATA2	ENET_TX_DATA2	GPIO_AD_B0_05	O
TXD3	TDATA3	ENET_TX_DATA3	GPIO_AD_B0_04	O
TX_EN	TX_EN	ENET_TX_EN	GPIO_EMC_24 GPIO_B1_09	O
TX_ER (optional)	TX_ER	ENET_TX_ER	GPIO_AD_B0_07	O
RX_CLK	RX_CLK	ENET_RX_CLK	GPIO_AD_B0_06	I
RXD0	RDATA0	ENET_RX_DATA0	GPIO_EMC_20 GPIO_B1_04	I
RXD1	RDATA1	ENET_RX_DATA1	GPIO_EMC_19 GPIO_B1_05	I
RXD2	RDATA2	ENET_RX_DATA2	GPIO_AD_B0_09	I
RXD3	RDATA3	ENET_RX_DATA3	GPIO_AD_B0_08	I
RX_DV	RX_EN	ENET_RX_EN	GPIO_EMC_23 GPIO_B1_06	I
RX_ER	RX_ER	ENET_RX_ER	GPIO_EMC_26 GPIO_B1_11	I
CRS	CRS	ENET_CRS	GPIO_AD_B0_10	I
COL	COL	ENET_COL	GPIO_AD_B0_11	I

Table 15. i.MX RT106x – ENET RMII pads

ENET		RMII		
General signal name	**MCU signal name**	**MCU port**	**MCU pin**	**Dir**
REF_CLK	REF_CLK1	ENET_REF_CLK	GPIO_EMC_25 GPIO_B1_10	I/O
TXD0	TDATA0	ENET_TX_DATA0	GPIO_EMC_22 GPIO_B1_07	O
TXD1	TDATA1	ENET_TX_DATA1	GPIO_EMC_21 GPIO_B1_08	O
TX_EN	TX_EN	ENET_TX_EN	GPIO_EMC_24 GPIO_B1_09	O
RXD0	RDATA0	ENET_RX_DATA0	GPIO_EMC_20 GPIO_B1_04	I
RXD1	RDATA1	ENET_RX_DATA1	GPIO_EMC_19 GPIO_B1_05	I
CRS_DV	RX_EN	ENET_RX_EN	GPIO_EMC_23 GPIO_B1_06	I
RX_ER	RX_ER	ENET_RX_ER	GPIO_EMC_26 GPIO_B1_11	I

Table 16. i.MX RT106x – ENET MDIO pads

ENET		MDIO		
General signal name	**MCU signal name**	**MCU port**	**MCU pin**	**Dir**
MDC	MDC	ENET_MDC	GPIO_EMC_40 GPIO_B1_14 GPIO_AD_B1_04	O
MDIO	MDIO	ENET_MDIO	GPIO_EMC_41 GPIO_B1_15 GPIO_AD_B1_05	I/O

4.3.2 ENET2 MII, RMII, and MDIO available pins

Table 17. i.MX RT106x – ENET2 MII pads

ENET2		MII		
General signal name	**MCU signal name**	**MCU port**	**MCU pin**	**Dir**
TX_CLK	TX_CLK	ENET2_TX_CLK	GPIO_EMC_33 GPIO_SD_B0_01 GPIO_B0_15	I
TXD0	TDATA0	ENET2_TX_DATA0	GPIO_EMC_30 GPIO_B0_12 GPIO_B1_14	O
TXD1	TDATA1	ENET2_TX_DATA1	GPIO_EMC_31 GPIO_B1_15	O

Table 17. i.MX RT106x – ENET2 MII pads *...continued*

ENET2		MII		
General signal name	**MCU signal name**	**MCU port**	**MCU pin**	**Dir**
			GPIO_B0_13	
TXD2	TDATA2	ENET2_TX_DATA2	GPIO_B0_05	O
TXD3	TDATA3	ENET2_TX_DATA3	GPIO_B0_04	O
TX_EN	TX_EN	ENET2_TX_EN	GPIO_EMC_32 GPIO_SD_B0_00 GPIO_B0_14	O
TX_ER (optional)	TX_ER	ENET2_TX_ER	GPIO_B0_07	O
RX_CLK	RX_CLK	ENET2_RX_CLK	GPIO_B0_06	I
RXD0	RDATA0	ENET2_RX_DATA0	GPIO_EMC_35 GPIO_SD_B0_03 GPIO_B1_01	I
RXD1	RDATA1	ENET2_RX_DATA1	GPIO_EMC_36 GPIO_SD_B0_04 GPIO_B1_02	I
RXD2	RDATA2	ENET2_RX_DATA2	GPIO_B0_09	I
RXD3	RDATA3	ENET2_RX_DATA3	GPIO_B0_08	I
RX_DV	RX_EN	ENET2_RX_EN	GPIO_EMC_37 GPIO_SD_B0_05 GPIO_B1_03	I
RX_ER	RX_ER	ENET2_RX_ER	GPIO_EMC_34 GPIO_SD_B0_02 GPIO_B1_00	I
CRS	CRS	ENET2_CRS	GPIO_B0_11	I
COL	COL	ENET2_COL	GPIO_B0_10	I

Table 18. i.MX RT106x – ENET2 MII pads

ENET2		RMII		
General signal name	**MCU signal name**	**MCU port name**	**MCU pin**	**Dir**
REF_CLK	REF_CLK1	ENET2_REF_CLK2	GPIO_EMC_33 GPIO_SD_B0_01 GPIO_B0_15	I/O
TXD0	TDATA0	ENET2_TX_DATA0	GPIO_EMC_30 GPIO_B1_14 GPIO_B0_12	O
TXD1	TDATA1	ENET2_TX_DATA1	GPIO_EMC_31 GPIO_B1_15 GPIO_B0_13	O
TX_EN	TX_EN	ENET2_TX_EN	GPIO_EMC_32 GPIO_SD_B0_00	O

Table 18. i.MX RT106x – ENET2 MII pads*...continued*

ENET2		RMII		
General signal name	**MCU signal name**	**MCU port name**	**MCU pin**	**Dir**
			GPIO_B0_14	
RXD0	RDATA0	ENET2_RX_DATA0	GPIO_EMC_35 GPIO_SD_B0_03 GPIO_B1_01	I
RXD1	RDATA1	ENET2_RX_DATA1	GPIO_EMC_36 GPIO_SD_B0_04 GPIO_B1_02	I
CRS_DV	RX_EN	ENET2_RX_EN	GPIO_EMC_37 GPIO_B1_03 GPIO_SD_B0_05	I
RX_ER	RX_ER	ENET2_RX_ER	GPIO_EMC_34 GPIO_B1_00 GPIO_SD_B0_02	I

Table 19. i.MX RT106x – ENET2 RMII pads

ENET2		MDIO		
General signal name	**MCU signal name**	**MCU port name**	**MCU pad**	**Dir**
MDC	MDC	ENET2_MDC	GPIO_EMC_40 GPIO_B1_14 GPIO_AD_B1_04	O
MDIO	MDIO	ENET2_MDIO	GPIO_EMC_41 GPIO_B1_15 GPIO_AD_B1_05	I/O

4.3.3 MII/RMII pin and clock configuration

According to the required connection (MII/RMII), select and configure one of the pins for each signal listed in Table 14 and Table 17(MII) or Table 15 and Table 18 (RMII). Do the same with the MDC and MDIO signals listed in Table 19.

The pin functionality is configured via the `SW_MUX_CTL_PAD_GPIO_n_SW MUX` control register. The pin direction is automatically determined by the selected functionality and it is listed in the column Dir.

Use the settings below for each selected pin and write the settings into the `SW_PAD_CTL_PAD_GPIO_n SW PAD` control register.

- Hysteresis – disabled
- Open Drain – disabled
- Speed - 150 MHz - 200 MHz
- Drive Strength - R0/5
- Slew Rate - Fast Slew Rate

Output pins (see the Dir column in the tables above):

- Pull Up / Down Config - 100 K ohm Pull Down (does not have effect)
- Pull / Keep Select – Keeper (does not have effect)

- Pull / Keep Enable - Pull/Keeper Disabled

Input pins (see the Dir column in the tables above):

- Pull Up / Down Config - 100 K ohm Pull Down
- Pull / Keep Select – Pull
- Pull / Keep Enable - Pull/Keeper Enabled

MDIO signal:

- Use the settings for input pins.

4.3.3.1 MII connection-specific settings

- Set the ENET1_TX_CLK_DIR bit in the IOMUXC_GPR_GPR1 register (if the ENET interface is used) to 0 that disables the ENET_TX_CLK output driver.
- Set the ENET1_CLK_SEL bit in the IOMUXC_GPR_GPR1 register (if the ENET interface is used) to 1. The TX_CLK reference is got from an external source.
- Set the ENET2_TX_CLK_DIR bit in the IOMUXC_GPR_GPR1 register (if the ENET2 interface is used) to 0 that disables the ENET2_TX_CLK output driver.
- Set the ENET2_CLK_SEL bit in the IOMUXC_GPR_GPR1 register (if the ENET2 interface is used) to 1. The TX_CLK reference is got from an external source.
- The ipg_clock_root frequency must be 25 MHz or higher.

4.3.3.2 RMII connection-specific settings

When the RMII connection is used, there are 2 possible ways to generate an RMII reference clock.

1. The RMII reference clock is provided by the MCU (the ENET_REF_CLK port is output). The following configurations must be used.
2. The RMII reference clock is provided by the 50 MHz external oscillator (the ENET_REF_CLK port is input).

The reference clock is provided by the MCU:

- Set the Sion bit in the SW_MUX_CTL_PAD_GPIO_n_SW MUX control register for the ENET_REF_CLK/ ENET2_REF_CLK2 pin to 1.
- Use the settings for output pins for ENET_REF_CLK/ENET2_REF_CLK2 in the SW_PAD_CTL_PAD_GPIO_n SW PAD control register.
- Enable the ENET_PLL output and set DIV_SELECT to 1. This is configured via the CCM_ANALOG_PLL_ENETn register. For the correct PLL initialization, read an appropriate chapter in the reference manual.
- Set the ENET1_TX_CLK_DIR bit in the IOMUXC_GPR_GPR1 register (if the ENET interface is used) or the ENET2_TX_CLK_DIR bit in the IOMUXC_GPR_GPR1 register (if the ENET2 interface is used) to 1 to enable the ENET_TX_CLK output driver.
- Set the ENET1_CLK_SEL bit in the IOMUXC_GPR_GPR1 register (if the ENET interface is used) or the ENET2_CLK_SEL bit in the IOMUXC_GPR_GPR1. register (if the ENET2 interface is used) to 0 to enable the reference clock to be driven by ENET_PLL.
- The ipg_clock_root frequency must be 50 MHz or higher.

The reference clock is provided by the 50 MHz external oscillator:

- Use the settings for input pins for ENET_REF_CLK/ENET2_REF_CLK2 in the SW_PAD_CTL_PAD_GPIO_n SW PAD control register.
- Set the ENET1_TX_CLK_DIR bit in the IOMUXC_GPR_GPR1 register (if the ENET interface is used) to 0. It disables the ENET_TX_CLK output driver.
- Set the ENET1_CLK_SEL bit in the IOMUXC_GPR_GPR1 register (if the ENET interface is used) to 1. The TX_CLK reference is got from an external source.

- Set the ENET2_TX_CLK_DIR bit in the IOMUXC_GPR_GPR1 register (if the ENET2 interface is used) to 0. It disables the ENET2_TX_CLK output driver.
- Set the ENET2_CLK_SEL bit in the IOMUXC_GPR_GPR1 register (if the ENET2 interface is used) to 1. The TX_CLK reference is got from an external source.
- The ipg_clock_root frequency must be 50 MHz or higher.

4.4 i.MX RT117x

The i.MX RT117x family provides one Fast Ethernet interface (ENET), one Gigabit Ethernet interface with AVB support (ENET1G) and one Gigabit Ethernet interface with AVB and TSN support called ENET_QoS. All three interfaces support the MII and RMII connection between the MAC and the PHY. Additionally, both Gigabit Ethernet interfaces support RGMII.

If no MII connection is used (only RMII and RGMII is used), all three interfaces can be used simultaneously. Each interface has to use a different set of pins. MDIO, MDC pins can be shared by more PHYs or each PHY can be connected to an individual pair of MDC, MDIO pins.

4.4.1 ENET MII, RMII, and MDIO available pins

Table 20. i.MX RT117x – ENET MII pads

ENET		MII		
General signal name	**MCU signal name**	**MCU port**	**MCU pin**	**Dir**
TX_CLK	TX_CLK	ENET_TX_CLK	GPIO_AD_29 GPIO_DISP_B2_05	I
TXD0	TX_DATA0	ENET_TX_DATA0	GPIO_AD_30 GPIO_DISP_B2_02	O
TXD1	TX_DATA1	ENET_TX_DATA1	GPIO_AD_31 GPIO_DISP_B2_03	O
TXD2	TX_DATA2	ENET_TX_DATA2	GPIO_AD_13	O
TXD3	TX_DATA3	ENET_TX_DATA3	GPIO_AD_12	O
TX_EN	TX_EN	ENET_TX_EN	GPIO_AD_28 GPIO_DISP_B2_04	O
TX_ER (optional)	TX_ER	ENET_TX_ER	GPIO_AD_15 GPIO_SD_B2_07	O
RX_CLK	RX_CLK	ENET_RX_CLK	GPIO_AD_14	I
RXD0	RX_DATA0	ENET_RX_DATA0	GPIO_AD_26 GPIO_DISP_B2_06	I
RXD1	RX_DATA1	ENET_RX_DATA1	GPIO_AD_27 GPIO_DISP_B2_07	I
RXD2	RX_DATA2	ENET_RX_DATA2	GPIO_AD_17	I
RXD3	RX_DATA3	ENET_RX_DATA3	GPIO_AD_16	I
RX_DV	RX_EN	ENET_RX_EN	GPIO_AD_24 GPIO_DISP_B2_08	I
RX_ER	RX_ER	ENET_RX_ER	GPIO_AD_25 GPIO_DISP_B2_09	I
CRS	CRS	ENET_CRS	GPIO_AD_18	I

Table 20. i.MX RT117x – ENET MII pads*...continued*

ENET		MII		
General signal name	MCU signal name	MCU port	MCU pin	Dir
COL	COL	ENET_COL	GPIO_AD_19	I

Table 21. i.MX RT117x – ENET RMII pads

ENET		RMII		
General signal name	MCU signal name	MCU port	MCU pin	Dir
REF_CLK	REF_CLK	ENET_REF_CLK	GPIO_AD_29 GPIO_DISP_B2_05 GPIO_DISP_B2_13	I/O
TXD0	TX_DATA0	ENET_TX_DATA0	GPIO_AD_30 GPIO_DISP_B2_02	O
TXD1	TX_DATA1	ENET_TX_DATA1	GPIO_AD_31 GPIO_DISP_B2_03	O
TX_EN	TX_EN	ENET_TX_EN	GPIO_AD_28 GPIO_DISP_B2_04	O
RXD0	RX_DATA0	ENET_RX_DATA0	GPIO_AD_26 GPIO_DISP_B2_06	I
RXD1	RX_DATA1	ENET_RX_DATA1	GPIO_AD_27 GPIO_DISP_B2_07	I
CRS_DV	RX_EN	ENET_RX_EN	GPIO_AD_24 GPIO_DISP_B2_08	I
RX_ER	RX_ER	ENET_RX_ER	GPIO_AD_25 GPIO_DISP_B2_09	I

Table 22. i.MX RT117x – ENET MDIO pads

ENET		MDIO		
General signal name	MCU signal name	MCU Port	MCU pin	Dir
MDC	MDC	ENET_MDC	GPIO_EMC_B2_19 GPIO_AD_32	O
MDIO	MDIO	ENET_MDIO	GPIO_EMC_B2_20 GPIO_AD_33	I/O

4.4.2 ENET MII/RMII pin and clock configuration

According to the required connection (MII/RMII), select and configure one of the pins for each signal listed in Table 20 (MII) or Table 21 (RMII). Do the same with the MDC and MDIO signals listed in Table 22.

The pin functionality is configured via the `SW_MUX_CTL_PAD_GPIO_n_SW MUX` control register. The pin direction is automatically determined by the selected functionality and it is listed in the column Dir.

Use the settings below for each selected pin and write the settings into the `SW_PAD_CTL_PAD_GPIO_n SW PAD` control register.

- Open Drain – disabled
- Drive Strength - high drive strength
- Slew Rate - Slow Slew Rate

Output pins (see the Dir column in the tables above):

- Pull / Keep Select – Pull Disable
- Pull Up / Down Config – Weak pull down (has no effect)

Input pins (see the Dir column in the tables above):

- Pull / Keep Select – Pull Enable
- Pull Up / Down Config – Weak pull down

MDIO signal:

- Use the settings for input pins.

4.4.2.1 MII connection-specific settings

- Set the ENET_TX_CLK_SEL bit in the IOMUXC_GPR_GPR4 register to 1. The TX_CLK reference is got from the pad.
- The BUS_CLOCK_ROOT frequency must be 25 MHz or higher.

4.4.2.2 RMII connection-specific settings

When the RMII connection is used, there are 2 possible ways to generate an RMII reference clock.

1. The RMII reference clock is provided by the MCU (the ENET_REF_CLK port is output).
2. The RMII reference clock is provided by the 50 MHz external oscillator (the ENET_REF_CLK port is input).

The RMII reference clock is provided by the MCU:

- Set the Sion bit in the SW_MUX_CTL_PAD_GPIO_n_SW MUX control register for the ENET_REF_CLK pin to 1.
- Use the settings for output pins for ENET_REF_CLK in the SW_PAD_CTL_PAD_GPIO_n SW PAD control register.
- Enable the SYS_PLL1_DIV2 output (500 MHz). For the correct PLL initialization, read an appropriate chapter in the reference manual.
- Configure the ENET1_CLOCK_ROOT source to 4 (SYS_PLL1_DIV2) and divider to 10. The clock root provides 50 MHz required by RMII.
- Set the ENET_REF_CLK_DIR bit in the IOMUXC_GPR_GPR4 register to 1 (ENET_REF_CLK is output driven by ENET1_CLK_ROOT).
- The BUS_CLOCK_ROOT frequency must be 50 MHz or higher.

The RMII reference clock is provided by the 50 MHz external oscillator:

- Use the settings for input pins for ENET_REF_CLK in the SW_PAD_CTL_PAD_GPIO_n SW PAD control register.
- Set the ENET_REF_CLK_DIR bit in the IOMUXC_GPR_GPR4 register to 0 (ENET_REF_CLK is input).
- The BUS_CLOCK_ROOT frequency must be 50 MHz or higher.

4.4.3 ENET1G MII, RMII, RGMII, and MDIO available pins

Table 23. i.MX RT117x – ENET1G MII pads

ENET1G		MII		
General signal name	MCU signal name	MCU port	MCU pin	Dir
TX_CLK	TX_CLK	ENET_1G_TX_CLK_IO	GPIO_EMC_B2_14 GPIO_DISP_B1_11 GPIO_SD_B2_11	I
TXD0	TX_DATA0	ENET_1G_TX_DATA0	GPIO_EMC_B2_11 GPIO_DISP_B1_09 GPIO_SD_B2_09	O
TXD1	TX_DATA1	ENET_1G_TX_DATA1	GPIO_EMC_B2_12 GPIO_DISP_B1_08 GPIO_SD_B2_08	O
TXD2	TX_DATA2	ENET_1G_TX_DATA2	GPIO_EMC_B2_04 GPIO_DISP_B1_07 GPIO_SD_B2_07	O
TXD3	TX_DATA3	ENET_1G_TX_DATA3	GPIO_EMC_B2_03 GPIO_SD_B2_06 GPIO_DISP_B1_06	O
TX_EN	TX_EN	ENET_1G_TX_EN	GPIO_EMC_B2_13 GPIO_DISP_B1_10 GPIO_SD_B2_10	O
TX_ER (optional)	TX_ER	ENET_1G_TX_ER	GPIO_EMC_B2_06 GPIO_DISP_B2_00	O
RX_CLK	RX_CLK	ENET_1G_RX_CLK	GPIO_EMC_B2_05 GPIO_DISP_B1_01 GPIO_SD_B2_01	I
RXD0	RX_DATA0	ENET_1G_RX_DATA0	GPIO_EMC_B2_15 GPIO_SD_B2_02 GPIO_DISP_B1_02	I
RXD1	RX_DATA1	ENET_1G_RX_DATA1	GPIO_EMC_B2_16 GPIO_SD_B2_03 GPIO_DISP_B1_03	I
RXD2	RX_DATA2	ENET_1G_RX_DATA2	GPIO_EMC_B2_08 GPIO_DISP_B1_04 GPIO_SD_B2_04	I
RXD3	RX_DATA3	ENET_1G_RX_DATA3	GPIO_EMC_B2_07 GPIO_SD_B2_05 GPIO_DISP_B1_05	I
RX_DV	RX_EN	ENET_1G_RX_EN	GPIO_EMC_B2_17 GPIO_SD_B2_00 GPIO_DISP_B1_00	I
RX_ER	RX_ER	ENET_1G_RX_ER	GPIO_EMC_B2_18 GPIO_DISP_B1_01	I

Table 23. i.MX RT117x – ENET1G MII pads*...continued*

ENET1G		MII		
General signal name	**MCU signal name**	**MCU port**	**MCU pin**	**Dir**
CRS	CRS	ENET_1G_CRS	GPIO_EMC_B2_09	I
COL	COL	ENET_1G_COL	GPIO_EMC_B2_10	I

Table 24. i.MX RT117x – ENET1G RMII pads

ENET1G		RMII		
General signal name	**MCU signal name**	**MCU port**	**MCU pin**	**Dir**
REF_CLK	REF_CLK	ENET_1G_REF_CLK	GPIO_EMC_B2_19 GPIO_DISP_B2_14 GPIO_DISP_B1_11 GPIO_SD_B2_11	I/O
TXD0	TX_DATA0	ENET_1G_TX_DATA0	GPIO_EMC_B2_11 GPIO_DISP_B1_09 GPIO_SD_B2_09	O
TXD1	TX_DATA1	ENET_1G_TX_DATA1	GPIO_EMC_B2_12 GPIO_SD_B2_08 GPIO_DISP_B1_08	O
TX_EN	TX_EN	ENET_1G_TX_EN	GPIO_EMC_B2_13 GPIO_SD_B2_10 GPIO_DISP_B1_10	O
RXD0	RX_DATA0	ENET_1G_RX_DATA0	GPIO_EMC_B2_15 GPIO_DISP_B1_02 GPIO_SD_B2_02	I
RXD1	RX_DATA1	ENET_1G_RX_DATA1	GPIO_EMC_B2_16 GPIO_DISP_B1_03 GPIO_SD_B2_03	I
CRS_DV	RX_EN	ENET_1G_RX_EN	GPIO_EMC_B2_17 GPIO_DISP_B1_00 GPIO_SD_B2_00	I
RX_ER	RX_ER	ENET_1G_RX_ER	GPIO_EMC_B2_18 GPIO_DISP_B1_01	I

Table 25. i.MX RT117x – ENET1G RGMII pads

ENET1G		RGMII		
General signal name	**MCU signal name**	**MCU port**	**MCU pin**	**Dir**
TXC	TX_CLK_IO	ENET_1G_TX_CLK_IO	GPIO_EMC_B2_14 GPIO_SD_B2_11 GPIO_DISP_B1_11	O
TXD0	TX_DATA0	ENET_1G_TX_DATA0	GPIO_EMC_B2_11 GPIO_DISP_B1_09	O

Table 25. i.MX RT117x – ENET1G RGMII pads*...continued*

ENET1G		RGMII		
General signal name	**MCU signal name**	**MCU port**	**MCU pin**	**Dir**
			GPIO_SD_B2_09	
TXD1	TX_DATA1	ENET_1G_TX_DATA1	GPIO_EMC_B2_12 GPIO_DISP_B1_08 GPIO_SD_B2_08	O
TXD2	TX_DATA2	ENET_1G_TX_DATA2	GPIO_EMC_B2_04 GPIO_SD_B2_07 GPIO_DISP_B1_07	O
TXD3	TX_DATA3	ENET_1G_TX_DATA3	GPIO_EMC_B2_03 GPIO_SD_B2_06 GPIO_DISP_B1_06	O
TX_CTL	TX_EN	ENET_1G_TX_EN	GPIO_EMC_B2_13 GPIO_DISP_B1_10 GPIO_SD_B2_10	O
RXC	RX_CLK	ENET_1G_RX_CLK	GPIO_EMC_B2_05 GPIO_SD_B2_01 GPIO_DISP_B1_01	I
RXD0	RX_DATA0	ENET_1G_RX_DATA0	GPIO_EMC_B2_15 GPIO_SD_B2_02 GPIO_DISP_B1_02	I
RXD1	RX_DATA1	ENET_1G_RX_DATA1	GPIO_EMC_B2_16 GPIO_SD_B2_03 GPIO_DISP_B1_03	I
RXD2	RX_DATA2	ENET_1G_RX_DATA2	GPIO_EMC_B2_08 GPIO_SD_B2_04 GPIO_DISP_B1_04	I
RXD3	RX_DATA3	ENET_1G_RX_DATA3	GPIO_EMC_B2_07 GPIO_SD_B2_05 GPIO_DISP_B1_05	I
RX_CTL	RX_EN	ENET_1G_RX_EN	GPIO_EMC_B2_17 GPIO_SD_B2_00 GPIO_DISP_B1_00	I

Table 26. i.MX RT117x – ENET1G MDIO pads

ENET1G		MDIO		
General signal name	**MCU signal name**	**MCU port**	**MCU pin**	**Dir**
MDC	MDC	ENET1G_MDC	GPIO_EMC_B2_19 GPIO_EMC_B1_40 GPIO_AD_16 GPIO_AD_32	O
MDIO	MDIO	ENET1G_MDIO	GPIO_EMC_B2_20 GPIO_EMC_B1_41	I/O

Table 26. i.MX RT117x – ENET1G MDIO pads...*continued*

ENET1G		MDIO		
General signal name	MCU signal name	MCU port	MCU pin	Dir
			GPIO_AD_17 GPIO_AD_33	

4.4.4 ENET1G MII/RMII/RGMII pin and clock configuration

According to the required connection (MII/RMII/RGMII), select and configure one of the pins for each signal listed in Table 23 (MII), Table 24 (RMII) or Table 25 (RGMII). Do the same with the MDC and MDIO signals listed in Table 26.

The pin functionality is configured via the SW_MUX_CTL_PAD_GPIO_n_SW MUX control register. The pin direction is automatically determined by the selected functionality and it is listed in the column Dir.

Use the settings below for each selected pin and write the settings into the SW_PAD_CTL_PAD_GPIO_n SW PAD control register.

- Open Drain – disabled
- PDRV - high drive strength

Output pins (see the Dir column in the tables above):

- Pull Down Pull Up – No Pull

Input pins (see the Dir column in the tables above):

- Pull Down Pull Up – Internal pulldown resistor enabled

MDIO signal:

- Use the settings for input pins.

4.4.4.1 MII connection-specific settings

- Set the ENET1G_TX_CLK_SEL bit in the IOMUXC_GPR_GPR5 register to 1. The TX_CLK reference is got from the pad.
- The BUS_CLOCK_ROOT frequency must be 25 MHz or higher.

4.4.4.2 RMII connection-specific settings

When the RMII connection is used, there are 2 possible ways to generate an RMII reference clock.

1. The RMII reference clock is provided by the MCU (the ENET_1G_REF_CLK port is output).
2. The RMII reference clock is provided by the 50 MHz external oscillator (the ENET_1G_REF_CLK port is input).

The RMII reference clock is provided by the MCU:

- Set the Sion bit in the SW_MUX_CTL_PAD_GPIO_n_SW MUX control register for the ENET_1G_REF_CLK pin to 1.
- Use the settings for output pins for ENET_1G_REF_CLK in the SW_PAD_CTL_PAD_GPIO_n SW PAD control register.
- Enable the SYS_PLL1_DIV2 output (500 MHz). For the correct PLL initialization, read an appropriate chapter in the reference manual.
- Configure the ENET2_CLOCK_ROOT source to 4 (SYS_PLL1_DIV2) and divider to 10. The clock root provides the 50 MHz required by RMII.

- Set the ENET1G_REF_CLK_DIR bit in the IOMUXC_GPR_GPR5 register to 1 (ENET1G_REF_CLK is output driven by ENET2_CLK_ROOT).
- The BUS_CLOCK_ROOT frequency must be 50 MHz or higher.

The RMII reference clock is provided by the 50 MHz external oscillator:

- Use the settings for input pins for ENET_1G_REF_CLK in the SW_PAD_CTL_PAD_GPIO_n SW PAD control register.
- Set the ENET1G_REF_CLK_DIR bit in the IOMUXC_GPR_GPR5 register to 0 (ENET1G_REF_CLK is input).
- The BUS_CLOCK_ROOT frequency must be 50 MHz or higher.

4.4.4.3 RGMII connection-specific settings

- Enable the SYS_PLL1_DIV2 output (500 MHz). For the correct PLL initialization, read an appropriate chapter in the reference manual.
- Configure the ENET2_CLOCK_ROOT source to 4 (SYS_PLL1_DIV2) and divider to 4. The clock root provides the 125 MHz required by RGMII.
- Set the ENET1G_TX_CLK_SEL bit in the IOMUXC_GPR_GPR5 register to 0. ENET1G TX_CLK is driven by ENET2_CLK_ROOT.
- Set the ENET1G_RGMII_EN bit in the IOMUXC_GPR_GPR5 register to 1. It enables the ENET1G RGMII TX clock output on the TX_CLK_IO pad.
- The BUS_CLOCK_ROOT frequency must be 125 MHz or higher.

4.4.5 ENET_QoS MII, RMII, RGMII, and MDIO available pins

Table 27. i.MX RT117x – ENET_QoS MII pads

ENET_QoS		MII		
General signal name	**MCU signal name**	**MCU port**	**MCU pin**	**Dir**
TX_CLK	TX_CLK	ENET_QOS_TX_CLK	GPIO_DISP_B2_05 GPIO_DISP_B1_11	I
TXD0	TX_DATA0	ENET_QOS_TX_DATA0	GPIO_DISP_B2_02 GPIO_DISP_B1_09	O
TXD1	TX_DATA1	ENET_QOS_TX_DATA1	GPIO_DISP_B2_03 GPIO_DISP_B1_08	O
TXD2	TX_DATA2	ENET_QOS_TX_DATA2	GPIO_DISP_B1_07	O
TXD3	TX_DATA3	ENET_QOS_TX_DATA3	GPIO_DISP_B1_06	O
TX_EN	TX_EN	ENET_QOS_TX_EN	GPIO_DISP_B2_04 GPIO_DISP_B1_10	O
TX_ER (optional)	TX_ER	ENET_QOS_TX_ER	GPIO_DISP_B2_00	O
RX_CLK	RX_CLK	ENET_QOS_RX_CLK	GPIO_DISP_B1_01	I
RXD0	RX_DATA0	ENET_QOS_RX_DATA0	GPIO_DISP_B2_06 GPIO_DISP_B1_02	I
RXD1	RX_DATA1	ENET_QOS_RX_DATA1	GPIO_DISP_B2_07 GPIO_DISP_B1_03	I
RXD2	RX_DATA2	ENET_QOS_RX_DATA2	GPIO_DISP_B1_04	I
RXD3	RX_DATA3	ENET_QOS_RX_DATA3	GPIO_DISP_B1_05	I
RX_DV	RX_EN	ENET_QOS_RX_EN	GPIO_DISP_B2_08	I

Table 27. i.MX RT117x – ENET_QoS MII pads*...continued*

ENET_QoS		MII		
General signal name	**MCU signal name**	**MCU port**	**MCU pin**	**Dir**
			GPIO_DISP_B1_00	
RX_ER	RX_ER	ENET_QOS_RX_ER	GPIO_DISP_B2_09 GPIO_DISP_B1_01 GPIO_DISP_B2_10	I
CRS	CRS	ENET_QOS_CRS	GPIO_DISP_B2_11	I
COL	COL	ENET_QOS_COL	GPIO_DISP_B2_12	I

Table 28. i.MX RT117x – ENET_QoS RMII pads

ENET_QoS		RMII		
General signal name	**MCU signal name**	**MCU port**	**MCU pin**	**Dir**
REF_CLK	REF_CLK	ENET_QOS_REF_CLK	GPIO_EMC_B2_20 GPIO_DISP_B1_11 GPIO_SD_B2_07	I/O
TXD0	TX_DATA0	ENET_QOS_TX_DATA0	GPIO_DISP_B2_02 GPIO_DISP_B1_09	O
TXD1	TX_DATA1	ENET_QOS_TX_DATA1	GPIO_DISP_B2_03 GPIO_DISP_B1_08	O
TX_EN	TX_EN	ENET_QOS_TX_EN	GPIO_DISP_B2_04 GPIO_DISP_B1_10	O
RXD0	RX_DATA0	ENET_QOS_RX_DATA0	GPIO_DISP_B2_06 GPIO_DISP_B1_02	I
RXD1	RX_DATA1	ENET_QOS_RX_DATA1	GPIO_DISP_B2_07 GPIO_DISP_B1_03	I
CRS_DV	RX_EN	ENET_QOS_RX_EN	GPIO_DISP_B2_08 GPIO_DISP_B1_00	I
RX_ER	RX_ER	ENET_QOS_RX_ER	GPIO_DISP_B2_09 GPIO_DISP_B1_01 GPIO_DISP_B2_10	I

Table 29. i.MX RT117x – ENET_QoS RGMII pads

ENET_QoS		RGMII		
General signal name	**MCU signal name**	**MCU port**	**MCU pin**	**Dir**
TXC	TX_CLK_IO	ENET_QOS_TX_CLK	GPIO_DISP_B2_05 GPIO_DISP_B1_11	O
TXD0	TX_DATA0	ENET_QOS_TX_DATA0	GPIO_DISP_B2_02 GPIO_DISP_B1_09	O
TXD1	TX_DATA1	ENET_QOS_TX_DATA1	GPIO_DISP_B2_03 GPIO_DISP_B1_08	O

Table 29. i.MX RT117x – ENET_QoS RGMII pads...*continued*

ENET_QoS		RGMII		
General signal name	**MCU signal name**	**MCU port**	**MCU pin**	**Dir**
TXD2	TX_DATA2	ENET_QOS_TX_DATA2	GPIO_DISP_B1_07	O
TXD3	TX_DATA3	ENET_QOS_TX_DATA3	GPIO_DISP_B1_06	O
TX_CTL	TX_EN	ENET_QOS_TX_EN	GPIO_DISP_B2_04 GPIO_DISP_B1_10	O
RXC	RX_CLK	ENET_QOS_RX_CLK	GPIO_DISP_B1_01	I
RXD0	RX_DATA0	ENET_QOS_RX_DATA0	GPIO_DISP_B2_06 GPIO_DISP_B1_02	I
RXD1	RX_DATA1	ENET_QOS_RX_DATA1	GPIO_DISP_B2_07 GPIO_DISP_B1_03	I
RXD2	RX_DATA2	ENET_QOS_RX_DATA2	GPIO_DISP_B1_04	I
RXD3	RX_DATA3	ENET_QOS_RX_DATA3	GPIO_DISP_B1_05	I
RX_CTL	RX_EN	ENET_QOS_RX_EN	GPIO_DISP_B2_08 GPIO_DISP_B1_00	I

Table 30. i.MX RT117x – ENET_QoS MDIO pads

ENET_QOS		MDIO		
General signal name	**MCU signal name**	**MCU port**	**MCU pin**	**Dir**
MDC	MDC	ENET_QOS_MDC	GPIO_EMC_B2_19 GPIO_AD_26	O
MDIO	MDIO	ENET_QOS_MDIO	GPIO_EMC_B2_20 GPIO_AD_27	I/O

4.4.6 ENET_QoS MII/RMII/RGMII pin and clock configuration

According to the required connection (MII/RMII/RGMII), select and configure one of the pins for each signal listed in Table 27 (MII), Table 28 (RMII) or Table 29 (RGMII). Do the same with the MDC and MDIO signals listed in Table 30.

The pin functionality is configured via the `SW_MUX_CTL_PAD_GPIO_n_SW MUX` control register. The pin direction is automatically determined by the selected functionality and it is listed in the column Dir.

Use the settings below for each selected `GPIO_DISP_B1_xx` or `GPIO_EMC_B2_xx` pin and write the settings into the `SW_PAD_CTL_PAD_GPIO_n SW PAD` control register.

- Open Drain – disabled
- PDRV - high drive strength

Output pins (see the Dir column in the tables above):

- Pull Down Pull Up – No Pull

Input pins (see the Dir column in the tables above):

- Pull Down Pull Up – Internal pulldown resistor enabled

MDIO signal:

- Use the settings for input pins.

For GPIO_DISP_B2_xx or GPIO_AD_xx pins, use the settings below:

- Open Drain – disabled
- Drive Strength - high drive strength
- Slew Rate - Slow Slew Rate

Output pins (see the Dir column in the tables above):

- Pull / Keep Select – Pull Disable
- Pull Up / Down Config – Weak pull down (has no effect)

Input pins (see the Dir column in the tables above):

- Pull / Keep Select – Pull Enable
- Pull Up / Down Config – Weak pull down

MDIO signal:

- Use the settings for input pins.

4.4.6.1 MII connection-specific settings

- Set the ENET_QOS_CLKGEN_EN bit in the IOMUXC_GPR_GPR6 register to 1. It enables the clock generator that provides the ENET_QOS TX/RX clocks according to the PHY interface type and speed.
- Set the ENET_QOS_INTF_SEL bit in the IOMUXC_GPR_GPR6 register to 0. It selects the MII interface.
- The BUS_CLOCK_ROOT frequency must be 25 MHz or higher.

4.4.6.2 RMII connection-specific settings

When the RMII connection is used, there are 2 possible ways to generate an RMII reference clock.

1. The RMII reference clock is provided by the MCU (the ENET_QOS_REF_CLK port is output).
2. The RMII reference clock is provided by the 50 MHz external oscillator (the ENET_QOS_REF_CLK port is input).

The RMII reference clock is provided by the MCU:

- Set the Sion bit in the SW_MUX_CTL_PAD_GPIO_n_SW MUX control register for the ENET_QOS_REF_CLK pin to 1.
- Use the settings for output pins for ENET_QOS_REF_CLK in the SW_PAD_CTL_PAD_GPIO_n SW PAD control register.
- Enable the SYS_PLL1_DIV2 output (500 MHz). For the correct PLL initialization, read an appropriate chapter in the reference manual.
- Configure the ENET_QOS_CLOCK_ROOT source to 4 (SYS_PLL1_DIV2) and divider to 10. The clock root provides the 50 MHz required by RMII.
- Set the ENET_QOS_INTF_SEL bit in the IOMUXC_GPR_GPR6 register to 4. It selects the RMII interface.
- Set the ENET_QOS_CLKGEN_EN bit in the IOMUXC_GPR_GPR6 register to 1. It enables the clock generator that provides the ENET_QOS TX/RX clocks according to the PHY interface type and speed.
- Set the ENET_QOS_REF_CLK_DIR bit in the IOMUXC_GPR_GPR6 register to 1 (ENET_QOS_REF_CLK is output-driven by ENET2_CLK_ROOT).
- The BUS_CLOCK_ROOT frequency must be 50 MHz or higher.

The RMII reference clock is provided by the 50 MHz external oscillator:

- Use the settings for input pins for ENET_QOS_REF_CLK in the SW_PAD_CTL_PAD_GPIO_n SW PAD control register.

- Set the ENET_QOS_INTF_SEL bit in the IOMUXC_GPR_GPR6 register to 4. It selects the RMII interface.
- Set the ENET_QOS_CLKGEN_EN bit in the IOMUXC_GPR_GPR6 register to 1. It enables the clock generator that provides the ENET_QOS TX/RX clocks according to the PHY interface type and speed.
- Set the ENET_QOS_REF_CLK_DIR bit in the IOMUXC_GPR_GPR6 register to 0 (ENET_QOS_REF_CLK is input).
- The BUS_CLOCK_ROOT frequency must be 50 MHz or higher.

4.4.6.3 RGMII connection-specific settings

- Enable the SYS_PLL1_DIV2 output (500 MHz). For the correct PLL initialization, read an appropriate chapter in the reference manual.
- Configure the ENET_QOS_CLOCK_ROOT source to 4 (SYS_PLL1_DIV2) and divider to 4. The clock root provides the 125 MHz required by RGMII.
- Set the ENET_QOS_INTF_SEL bit in the IOMUXC_GPR_GPR6 register to 1. It selects the RGMII interface.
- Set the ENET_QOS_RGMII_EN bit in the IOMUXC_GPR_GPR6 register to 1. It enables the ENET_QOS RGMII TX clock output on the TX_CLK pad.
- The BUS_CLOCK_ROOT frequency must be 125 MHz or higher.

4.5 i.MX RT118x

The i.MX RT118x family provides one NETC controller that consists of a 5-Gigabit port switch and two Gigabit Ethernet controllers (ENETC0/1).

The ENETC1 controller is internally connected to the switch port using a Pseudo MAC interface. The rest of the ports (four switch ports and one Ethernet controller port) are routed outside the MCU. All 5 ports support MII, RMII, and RGMII between the MAC and the PHY. ETH0 – ETH3 are interfaces for switch ports. ETH4 is an ENETC0 interface.

If no MII connection is used (only RMII and RGMII are used), all 5 interfaces can be used simultaneously. Each interface has to use a different set of pins. MDIO and MDC pins can be shared by more PHYs or each PHY can be connected to an individual pair of MDC, MDIO pins.

4.5.1 ETH0 MII, RMII, and RGMII available pins

Table 31. i.MX RT1180 - ETH0 MII pads

ETH0		MII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
TX_CLK	TX_CLK	ETH0_TX_CLK	GPIO_EMC_B1_37 GPIO_EMC_B2_08	I
TXD0	TX_DATA0	ETH0_TX_DATA0	GPIO_EMC_B1_34 GPIO_EMC_B2_05	O
TXD1	TX_DATA1	ETH0_TX_DATA1	GPIO_EMC_B1_35 GPIO_EMC_B2_06	O
TXD2	TX_DATA2	ETH0_TX_DATA2	GPIO_EMC_B2_03 GPIO_EMC_B2_14	O
TXD3	TX_DATA3	ETH0_TX_DATA3	GPIO_EMC_B2_04 GPIO_EMC_B2_13	O
TX_EN	TX_EN	ETH0_TX_EN	GPIO_EMC_B1_36 GPIO_EMC_B2_07	O
TX_ER (optional)	TX_ER	ETH0_TX_ER	GPIO_EMC_B2_18	O

Table 31. i.MX RT1180 - ETH0 MII pads*...continued*

ETH0		MII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
RX_CLK	RX_CLK	ETH0_RX_CLK	GPIO_EMC_B2_00 GPIO_EMC_B2_15	I
RXD0	RX_DATA0	ETH0_RX_DATA0	GPIO_EMC_B1_38 GPIO_EMC_B2_09	I
RXD1	RX_DATA1	ETH0_RX_DATA1	GPIO_EMC_B1_39 GPIO_EMC_B2_10	I
RXD2	RX_DATA2	ETH0_RX_DATA2	GPIO_EMC_B2_01 GPIO_EMC_B2_16	I
RXD3	RX_DATA3	ETH0_RX_DATA3	GPIO_EMC_B2_02 GPIO_EMC_B2_17	I
RX_DV	RX_EN	ETH0_RX_EN	GPIO_EMC_B1_40 GPIO_EMC_B2_11	I
RX_ER	RX_ER	ETH0_RX_ER	GPIO_EMC_B1_41 GPIO_EMC_B2_12	I
CRS	CRS	ETH0_CRS	GPIO_EMC_B2_19	I
COL	COL	ETH0_COL	GPIO_EMC_B2_20	I

Table 32. i.MX RT1180 - ETH0 RMII pads

ETH0		RMII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
REF_CLK	TX_CLK	ETH0_TX_CLK	GPIO_EMC_B1_37 GPIO_EMC_B2_08	I/O
TXD0	TX_DATA0	ETH0_TX_DATA0	GPIO_EMC_B1_34 GPIO_EMC_B2_05	O
TXD1	TX_DATA1	ETH0_TX_DATA1	GPIO_EMC_B1_35 GPIO_EMC_B2_06	O
TX_EN	TX_EN	ETH0_TX_EN	GPIO_EMC_B1_36 GPIO_EMC_B2_07	O
RXD0	RX_DATA0	ETH0_RX_DATA0	GPIO_EMC_B1_38 GPIO_EMC_B2_09	I
RXD1	RX_DATA1	ETH0_RX_DATA1	GPIO_EMC_B1_39 GPIO_EMC_B2_10	I
CRS_DV	RX_EN	ETH0_RX_EN	GPIO_EMC_B1_40 GPIO_EMC_B2_11	I
RX_ER	RX_ER	ETH0_RX_ER	GPIO_EMC_B1_41 GPIO_EMC_B2_12	I

Table 33. i.MX RT1180 - ETH0 RGMII pads

ETH0		RGMII		
General signal name	MCU signal name	Port	MCU pin	Dir
TXC	TX_CLK	ETH0_TX_CLK	GPIO_EMC_B1_37 GPIO_EMC_B2_08	O
TXD0	TX_DATA0	ETH0_TX_DATA0	GPIO_EMC_B1_34 GPIO_EMC_B2_05	O
TXD1	TX_DATA1	ETH0_TX_DATA1	GPIO_EMC_B1_35 GPIO_EMC_B2_06	O
TXD2	TX_DATA2	ETH0_TX_DATA2	GPIO_EMC_B2_03 GPIO_EMC_B2_14	O
TXD3	TX_DATA3	ETH0_TX_DATA3	GPIO_EMC_B2_04 GPIO_EMC_B2_13	O
TX_CTL	TX_EN	ETH0_TX_EN	GPIO_EMC_B1_36 GPIO_EMC_B2_07	O
RXC	RX_CLK	ETH0_RX_CLK	GPIO_EMC_B2_00 GPIO_EMC_B2_15	I
RXD0	RX_DATA0	ETH0_RX_DATA0	GPIO_EMC_B1_38 GPIO_EMC_B2_09	I
RXD1	RX_DATA1	ETH0_RX_DATA1	GPIO_EMC_B1_39 GPIO_EMC_B2_10	I
RXD2	RX_DATA2	ETH0_RX_DATA2	GPIO_EMC_B2_01 GPIO_EMC_B2_16	I
RXD3	RX_DATA3	ETH0_RX_DATA3	GPIO_EMC_B2_02 GPIO_EMC_B2_17	I
RX_CTL	RX_EN	ETH0_RX_EN	GPIO_EMC_B1_40 GPIO_EMC_B2_11	I

4.5.2 ETH0 MII/RMII/RGMII pin and clock configuration

According to the required connection (MII/RMII/RGMII), select and configure one of the pins for each signal listed in Table 31 (MII), Table 32 (RMII) or Table 33 (RGMII).

The pin functionality is configured via the `SW_MUX_CTL_PAD_GPIO_n_SW MUX` control register. The pin direction is automatically determined by the selected functionality and it is listed in the column Dir.

Use the settings below for each selected pin and write the settings into the `SW_PAD_CTL_PAD_GPIO_n SW PAD` control register.

- Open Drain – disabled
- PDRV - high drive strength

Output pins (see the Dir column in the tables above):

- Pull Down Pull Up – No Pull

Input pins (see the Dir column in the tables above):

- Pull Down Pull Up – PD

4.5.2.1 MII connection-specific settings

- Set the MII_PROT bit in the NETC_LINK_CFG0 register to 0 (MII).
- The NETC_CLOCK_ROOT frequency must be 25 MHz or higher.

4.5.2.2 RMII connection-specific settings

When the RMII connection is used, there are 2 possible ways to generate an RMII reference clock.

1. The RMII reference clock is provided by the MCU (the ETH0_TX_CLK port is output).
2. The RMII reference clock is provided by the 50 MHz external oscillator (the ETH0_TX_CLK port is input)

The RMII reference clock is provided by the MCU:

- Set the Sion bit in the SW_MUX_CTL_PAD_GPIO_n_SW MUX control register for the ETH0_TX_CLK pin to 1.
- Set the MII_PROT bit in the NETC_LINK_CFG0 register to 1 (RMII).
- Set the PORT0_RMII_REF_CLK_DIR bit in the NETC_PORT_MISC_CFG register to 1 (the Port0 RMII reference clock is output).
- Use the settings for output pins for the ETH0_TX_CLK in the SW_PAD_CTL_PAD_GPIO_n SW PAD control register.
- Enable the SYS_PLL1_DIV2 output (500 MHz). For the correct PLL initialization, read an appropriate chapter in the reference manual.
- Configure the MAC0_CLOCK_ROOT source to 2 (SYS_PLL1_DIV2) and divider to 10. The clock root provides 50 MHz required by RMII.
- The NETC_CLOCK_ROOT frequency must be 50 MHz or higher.

The RMII reference clock is provided by the 50 MHz external oscillator:

- Use the settings for input pins for the ETH0_TX_CLK in SW_PAD_CTL_PAD_GPIO_n SW PAD control register.
- Set the PORT0_RMII_REF_CLK_DIR bit in the NETC_PORT_MISC_CFG register to 0 (the Port0 RMII reference clock is input).
- The NETC_CLOCK_ROOT frequency must be 50 MHz or higher.

4.5.2.3 RGMII connection-specific settings

- Enable the SYS_PLL1_DIV2 output (500 MHz). For the correct PLL initialization, read an appropriate chapter in the reference manual.
- Configure the MAC0_CLOCK_ROOT source to 2 (SYS_PLL1_DIV2) and divider to 4. The clock root provides the 125 MHz required by RGMII.
- Set the MII_PROT bit in the NETC_LINK_CFG0 register to 2 (RGMII).
- The NETC_CLOCK_ROOT frequency must be 125 MHz or higher

4.5.3 ETH1 MII, RMII, and RGMII available pins

Table 34. i.MX RT1180 – ETH1 MII pads

ETH1		MII		
General signal name	MCU signal name	Port	MCU pin	Dir
TX_CLK	TX_CLK	ETH1_TX_CLK	GPIO_B1_03	I
TXD0	TX_DATA0	ETH1_TX_DATA0	GPIO_B1_00	O
TXD1	TX_DATA1	ETH1_TX_DATA1	GPIO_B1_01	O
TXD2	TX_DATA2	ETH1_TX_DATA2	GPIO_B1_07	O

Table 34. i.MX RT1180 – ETH1 MII pads*...continued*

ETH1		MII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
TXD3	TX_DATA3	ETH1_TX_DATA3	GPIO_B1_08	O
TX_EN	TX_EN	ETH1_TX_EN	GPIO_B1_02	O
TX_ER (optional)	TX_ER	ETH1_TX_ER	GPIO_B1_13	O
RX_CLK	RX_CLK	ETH1_RX_CLK	GPIO_B1_11	I
RXD0	RX_DATA0	ETH1_RX_DATA0	GPIO_B1_04	I
RXD1	RX_DATA1	ETH1_RX_DATA1	GPIO_B1_05	I
RXD2	RX_DATA2	ETH1_RX_DATA2	GPIO_B1_09	I
RXD3	RX_DATA3	ETH1_RX_DATA3	GPIO_B1_10	I
RX_DV	RX_EN	ETH1_RX_EN	GPIO_B1_06	I
RX_ER	RX_ER	ETH1_RX_ER	GPIO_B1_12	I
CRS	CRS	ETH1_CRS	GPIO_B2_00	I
COL	COL	ETH1_COL	GPIO_B2_01	I

Table 35. i.MX RT1180 – ETH1 RMII pads

ETH1		RMII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
REF_CLK	TX_CLK	ETH1_TX_CLK	GPIO_B1_03	I/O
TXD0	TX_DATA0	ETH1_TX_DATA0	GPIO_B1_00	O
TXD1	TX_DATA1	ETH1_TX_DATA1	GPIO_B1_01	O
TX_EN	TX_EN	ETH1_TX_EN	GPIO_B1_02	O
RXD0	RX_DATA0	ETH1_RX_DATA0	GPIO_B1_04	I
RXD1	RX_DATA1	ETH1_RX_DATA1	GPIO_B1_05	I
CRS_DV	RX_EN	ETH1_RX_EN	GPIO_B1_06	I
RX_ER	RX_ER	ETH1_RX_ER	GPIO_B1_12	I

Table 36. i.MX RT1180 – ETH1 RGMII pads

ETH1		RGMII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
TXC	TX_CLK	ETH1_TX_CLK	GPIO_B1_03	O
TXD0	TX_DATA0	ETH1_TX_DATA0	GPIO_B1_00	O
TXD1	TX_DATA1	ETH1_TX_DATA1	GPIO_B1_01	O
TXD2	TX_DATA2	ETH1_TX_DATA2	GPIO_B1_07	O
TXD3	TX_DATA3	ETH1_TX_DATA3	GPIO_B1_08	O
TX_CTL	TX_EN	ETH1_TX_EN	GPIO_B1_02	O

Table 36. i.MX RT1180 – ETH1 RGMII pads...*continued*

ETH1		RGMII		
General signal name	MCU signal name	Port	MCU pin	Dir
RXC	RX_CLK	ETH1_RX_CLK	GPIO_B1_11	I
RXD0	RX_DATA0	ETH1_RX_DATA0	GPIO_B1_04	I
RXD1	RX_DATA1	ETH1_RX_DATA1	GPIO_B1_05	I
RXD2	RX_DATA2	ETH1_RX_DATA2	GPIO_B1_09	I
RXD3	RX_DATA3	ETH1_RX_DATA3	GPIO_B1_10	I
RX_CTL	RX_EN	ETH1_RX_EN	GPIO_B1_06	I

4.5.4 ETH1 MII/RMII/RGMII pin and clock configuration

According to the required connection (MII/RMII/RGMII), select and configure one of the pins for each signal listed in Table 34 (MII), Table 35 (RMII) or Table 36 (RGMII).

The pin functionality is configured via the `SW_MUX_CTL_PAD_GPIO_n_SW MUX` control register. The pin direction is automatically determined by the selected functionality and it is listed in the column Dir.

Use the settings below for each selected pin and write the settings into the `SW_PAD_CTL_PAD_GPIO_n SW PAD` control register.

- Open Drain – disabled
- PDRV - high drive strength

Output pins (see the Dir column in the tables above):

- Pull Down Pull Up – No Pull

Input pins (see the Dir column in the tables above):

- Pull Down Pull Up – PD

4.5.4.1 MII connection-specific settings

- Set the `MII_PROT` bit in the `NETC_LINK_CFG1` register to 0 (MII).
- The `NETC_CLOCK_ROOT` frequency must be 25 MHz or higher.

4.5.4.2 RMII connection-specific settings

When the RMII connection is used, there are 2 possible ways to generate an RMII reference clock.

1. The RMII reference clock is provided by the MCU (the `ETH1_TX_CLK` port is output).
2. The RMII reference clock is provided by the 50 MHz external oscillator (the `ETH1_TX_CLK` port is input).

The RMII reference clock is provided by the MCU:

- Set the Sion bit in the `SW_MUX_CTL_PAD_GPIO_n_SW MUX` control register for the `ETH1_TX_CLK` pin to 1.
- Set the `MII_PROT` bit in the `NETC_LINK_CFG1` register to 1 (RMII).
- Set the `PORT1_RMII_REF_CLK_DIR` bit in the `NETC_PORT_MISC_CFG` register to 1 (the Port1 RMII reference clock is output).
- Use the settings for output pins for `ETH1_TX_CLK` in the `SW_PAD_CTL_PAD_GPIO_n SW PAD` control register.
- Enable the `SYS_PLL1_DIV2` output (500 MHz). For the correct PLL initialization, read an appropriate chapter in the reference manual.

- Configure the MAC1_CLOCK_ROOT source to 2 (SYS_PLL1_DIV2) and divider to 10. The clock root provides the 50 MHz required by RMII.
- The NETC_CLOCK_ROOT frequency must be 50 MHz or higher.

The RMII reference clock is provided by the 50 MHz external oscillator:

- Use the settings for input pins for ETH1_TX_CLK in the SW_PAD_CTL_PAD_GPIO_n SW PAD control register.
- Set the PORT1_RMII_REF_CLK_DIR bit in the NETC_PORT_MISC_CFG register to 0 (the Port1 RMII reference clock is input).
- The NETC_CLOCK_ROOT frequency must be 50 MHz or higher.

4.5.4.3 RGMII connection-specific settings

- Enable the SYS_PLL1_DIV2 output (500 MHz). For the correct PLL initialization, read an appropriate chapter in the reference manual.
- Configure the MAC1_CLOCK_ROOT source to 2 (SYS_PLL1_DIV2) and divider to 4. The clock root provides the 125 MHz required by RGMII.
- Set the MII_PROT bit in the NETC_LINK_CFG1 register to 2 (RGMII).
- The NETC_CLOCK_ROOT frequency must be 125 MHz or higher.

4.5.5 ETH2 MII, RMII, and RGMII available pins

Table 37. i.MX RT1180 – ETH2 MII pads

ETH2		MII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
TX_CLK	TX_CLK	ETH2_TX_CLK	GPIO_EMC_B1_15 GPIO_EMC_B1_29 GPIO_B2_09	I
TXD0	TX_DATA0	ETH2_TX_DATA0	GPIO_EMC_B1_27 GPIO_B2_06	O
TXD1	TX_DATA1	ETH2_TX_DATA1	GPIO_EMC_B1_26 GPIO_B2_07	O
TXD2	TX_DATA2	ETH2_TX_DATA2	GPIO_EMC_B1_25 GPIO_EMC_B1_37 GPIO_B2_04	O
TXD3	TX_DATA3	ETH2_TX_DATA3	GPIO_EMC_B1_24 GPIO_EMC_B1_36 GPIO_B2_05	O
TX_EN	TX_EN	ETH2_TX_EN	GPIO_EMC_B1_14 GPIO_EMC_B1_28 GPIO_B2_08	O
TX_ER (optional)	TX_ER	ETH2_TX_ER	GPIO_EMC_B1_20 GPIO_EMC_B1_39	O
RX_CLK	RX_CLK	ETH2_RX_CLK	GPIO_EMC_B1_21 GPIO_EMC_B1_33 GPIO_EMC_B1_38 GPIO_B2_13	I
RXD0	RX_DATA0	ETH2_RX_DATA0	GPIO_EMC_B1_16	I

Table 37. i.MX RT1180 – ETH2 MII pads*...continued*

ETH2		MII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
			GPIO_EMC_B1_30 GPIO_B2_10	
RXD1	RX_DATA1	ETH2_RX_DATA1	GPIO_EMC_B1_17 GPIO_EMC_B1_31 GPIO_B2_11	I
RXD2	RX_DATA2	ETH2_RX_DATA2	GPIO_EMC_B1_22 GPIO_EMC_B1_34 GPIO_B2_02	I
RXD3	RX_DATA3	ETH2_RX_DATA3	GPIO_EMC_B1_23 GPIO_EMC_B1_35 GPIO_B2_03	I
RX_DV	RX_EN	ETH2_RX_EN	GPIO_EMC_B1_13 GPIO_EMC_B1_32 GPIO_B2_12	I
RX_ER	RX_ER	ETH2_RX_ER	GPIO_EMC_B1_33 GPIO_B2_01	I
CRS	CRS	ETH2_CRS	GPIO_EMC_B1_18 GPIO_EMC_B1_40	I
COL	COL	ETH2_COL	GPIO_EMC_B1_19 GPIO_EMC_B1_41	I

Table 38. i.MX RT1180 – ETH2 RMII pads

ETH2		RMII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
REF_CLK	TX_CLK	ETH2_TX_CLK	GPIO_EMC_B1_15 GPIO_B2_09 GPIO_EMC_B1_29	I/O
TXD0	TX_DATA0	ETH2_TX_DATA0	GPIO_EMC_B1_27 GPIO_B2_06	O
TXD1	TX_DATA1	ETH2_TX_DATA1	GPIO_EMC_B1_26 GPIO_B2_07	O
TX_EN	TX_EN	ETH2_TX_EN	GPIO_EMC_B1_14 GPIO_EMC_B1_28 GPIO_B2_08	O
RXD0	RX_DATA0	ETH2_RX_DATA0	GPIO_EMC_B1_16 GPIO_EMC_B1_30 GPIO_B2_10	I
RXD1	RX_DATA1	ETH2_RX_DATA1	GPIO_EMC_B1_17 GPIO_EMC_B1_31 GPIO_B2_11	I

Table 38. i.MX RT1180 – ETH2 RMII pads*...continued*

ETH2		RMII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
CRS_DV	RX_EN	ETH2_RX_EN	GPIO_EMC_B1_13 GPIO_EMC_B1_32 GPIO_B2_12	I
RX_ER	RX_ER	ETH2_RX_ER	GPIO_EMC_B1_33 GPIO_B2_01	I

Table 39. i.MX RT1180 – ETH2 RGMII pads

ETH2		RGMII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
TXC	TX_CLK	ETH2_TX_CLK	GPIO_EMC_B1_15 GPIO_EMC_B1_29 GPIO_B2_09	O
TXD0	TX_DATA0	ETH2_TX_DATA0	GPIO_EMC_B1_27 GPIO_B2_06	O
TXD1	TX_DATA1	ETH2_TX_DATA1	GPIO_EMC_B1_26 GPIO_B2_07	O
TXD2	TX_DATA2	ETH2_TX_DATA2	GPIO_EMC_B1_25 GPIO_EMC_B1_37 GPIO_B2_04	O
TXD3	TX_DATA3	ETH2_TX_DATA3	GPIO_EMC_B1_24 GPIO_EMC_B1_36 GPIO_B2_05	O
TX_CTL	TX_EN	ETH2_TX_EN	GPIO_EMC_B1_14 GPIO_EMC_B1_28 GPIO_B2_08	O
RXC	RX_CLK	ETH2_RX_CLK	GPIO_EMC_B1_21 GPIO_EMC_B1_33 GPIO_EMC_B1_38 GPIO_B2_13	I
RXD0	RX_DATA0	ETH2_RX_DATA0	GPIO_EMC_B1_16 GPIO_EMC_B1_30 GPIO_B2_10	I
RXD1	RX_DATA1	ETH2_RX_DATA1	GPIO_EMC_B1_17 GPIO_EMC_B1_31 GPIO_B2_11	I
RXD2	RX_DATA2	ETH2_RX_DATA2	GPIO_EMC_B1_22 GPIO_EMC_B1_34 GPIO_B2_02	I
RXD3	RX_DATA3	ETH2_RX_DATA3	GPIO_EMC_B1_23 GPIO_EMC_B1_35 GPIO_B2_03	I

Table 39. i.MX RT1180 – ETH2 RGMII pads...*continued*

ETH2		RGMII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
RX_CTL	RX_EN	ETH2_RX_EN	GPIO_EMC_B1_13 GPIO_EMC_B1_32 GPIO_B2_12	I

4.5.6 ETH2 MII/RMII/RGMII pin and clock configuration

According to the required connection (MII/RMII/RGMII), select and configure one of the pins for each signal listed in Table 37 (MII), Table 38 (RMII) or Table 39 (RGMII).

The pin functionality is configured via the `SW_MUX_CTL_PAD_GPIO_n_SW MUX` control register. The pin direction is automatically determined by the selected functionality and it is listed in the column Dir.

Use the settings below for each selected pin and write the settings into the `SW_PAD_CTL_PAD_GPIO_n SW PAD` control register.

- Open Drain – disabled
- PDRV - high drive strength

Output pins (see the Dir column in the tables above):

- Pull Down Pull Up – No Pull

Input pins (see the Dir column in the tables above):

- Pull Down Pull Up – PD

4.5.6.1 MII connection-specific settings

- Set the `MII_PROT` bit in the `NETC_LINK_CFG2` register to 0 (MII).
- The `NETC_CLOCK_ROOT` frequency must be 25 MHz or higher.

4.5.6.2 RMII connection-specific settings

When the RMII connection is used, there are 2 possible ways to generate an RMII reference clock.

1. The RMII reference clock is provided by the MCU (the `ETH2_TX_CLK` port is output).
2. The RMII reference clock is provided by the 50 MHz external oscillator (the `ETH2_TX_CLK` port is input)

The RMII reference clock is provided by the MCU:

- Set the Sion bit in the `SW_MUX_CTL_PAD_GPIO_n_SW MUX` control register for the `ETH2_TX_CLK` pin to 1.
- Set the `MII_PROT` bit in the `NETC_LINK_CFG2` register to 1 (RMII).
- Set the `PORT2_RMII_REF_CLK_DIR` bit in the `NETC_PORT_MISC_CFG` register to 1 (the Port2 RMII reference clock is output).
- Use the settings for output pins for `ETH2_TX_CLK` in the `SW_PAD_CTL_PAD_GPIO_n SW PAD` control register
- Enable the `SYS_PLL1_DIV2` output (500 MHz). For the correct PLL initialization, read an appropriate chapter in the reference manual.
- Configure the `MAC2_CLOCK_ROOT` source to 2 (`SYS_PLL1_DIV2`) and divider to 10. The clock root provides the 50 MHz required by RMII.
- The `NETC_CLOCK_ROOT` frequency must be 50 MHz or higher.

The RMII reference clock is provided by the 50 MHz external oscillator:

- Use the settings for input pins for ETH2_TX_CLK in the SW_PAD_CTL_PAD_GPIO_n SW PAD control register.
- Set the PORT2_RMII_REF_CLK_DIR bit in the NETC_PORT_MISC_CFG register to 0 (the Port2 RMII reference clock is input).
- The NETC_CLOCK_ROOT frequency must be 50 MHz or higher.

4.5.6.3 RGMII connection-specific settings

- Enable the SYS_PLL1_DIV2 output (500 MHz). For the correct PLL initialization, read an appropriate chapter in the reference manual.
- Configure the MAC2_CLOCK_ROOT source to 2 (SYS_PLL1_DIV2) and divider to 4. The clock root provides the 125 MHz required by RGMII.
- Set the MII_PROT bit in the NETC_LINK_CFG2 register to 2 (RGMII).
- The NETC_CLOCK_ROOT frequency must be 125 MHz or higher.

4.5.7 ETH3 MII, RMII, and RGMII available pins

Table 40. i.MX RT1180 – ETH3 MII pads

ETH3		MII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
TX_CLK	TX_CLK	ETH3_TX_CLK	GPIO_EMC_B1_08 GPIO_EMC_B2_08	I
TXD0	TX_DATA0	ETH3_TX_DATA0	GPIO_EMC_B1_05 GPIO_EMC_B2_05	O
TXD1	TX_DATA1	ETH3_TX_DATA1	GPIO_EMC_B1_06 GPIO_EMC_B2_06	O
TXD2	TX_DATA2	ETH3_TX_DATA2	GPIO_EMC_B1_01 GPIO_EMC_B2_14	O
TXD3	TX_DATA3	ETH3_TX_DATA3	GPIO_EMC_B1_00 GPIO_EMC_B2_13	O
TX_EN	TX_EN	ETH3_TX_EN	GPIO_EMC_B1_07 GPIO_EMC_B2_07	O
TX_ER (optional)	TX_ER	ETH3_TX_ER	GPIO_EMC_B1_13 GPIO_EMC_B2_18	O
RX_CLK	RX_CLK	ETH3_RX_CLK	GPIO_EMC_B1_02 GPIO_EMC_B2_15	I
RXD0	RX_DATA0	ETH3_RX_DATA0	GPIO_EMC_B1_09 GPIO_EMC_B2_09	I
RXD1	RX_DATA1	ETH3_RX_DATA1	GPIO_EMC_B1_10 GPIO_EMC_B2_10	I
RXD2	RX_DATA2	ETH3_RX_DATA2	GPIO_EMC_B1_04 GPIO_EMC_B2_16	I
RXD3	RX_DATA3	ETH3_RX_DATA3	GPIO_EMC_B1_03 GPIO_EMC_B2_17	I
RX_DV	RX_EN	ETH3_RX_EN	GPIO_EMC_B1_11 GPIO_EMC_B2_11	I

Table 40. i.MX RT1180 – ETH3 MII pads*...continued*

ETH3		MII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
RX_ER	RX_ER	ETH3_RX_ER	GPIO_EMC_B1_12 GPIO_EMC_B2_12	I
CRS	CRS	ETH3_CRS	GPIO_EMC_B1_14 GPIO_EMC_B2_03	I
COL	COL	ETH3_COL	GPIO_EMC_B1_15 GPIO_EMC_B2_04	I

Table 41. i.MX RT1180 – ETH3 RMII pads

ETH3		RMII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
REF_CLK	TX_CLK	ETH3_TX_CLK	GPIO_EMC_B1_08 GPIO_EMC_B2_08	I/O
TXD0	TX_DATA0	ETH3_TX_DATA0	GPIO_EMC_B1_05 GPIO_EMC_B2_05	O
TXD1	TX_DATA1	ETH3_TX_DATA1	GPIO_EMC_B1_06 GPIO_EMC_B2_06	O
TX_EN	TX_EN	ETH3_TX_EN	GPIO_EMC_B1_07 GPIO_EMC_B2_07	O
RXD0	RX_DATA0	ETH3_RX_DATA0	GPIO_EMC_B1_09 GPIO_EMC_B2_09	I
RXD1	RX_DATA1	ETH3_RX_DATA1	GPIO_EMC_B1_10 GPIO_EMC_B2_10	I
CRS_DV	RX_EN	ETH3_RX_EN	GPIO_EMC_B1_11 GPIO_EMC_B2_11	I
RX_ER	RX_ER	ETH3_RX_ER	GPIO_EMC_B1_12 GPIO_EMC_B2_12	I

Table 42. i.MX RT1180 – ETH3 RGMII pads

ETH3		RGMII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
TXC	TX_CLK	ETH3_TX_CLK	GPIO_EMC_B1_08 GPIO_EMC_B2_08	O
TXD0	TX_DATA0	ETH3_TX_DATA0	GPIO_EMC_B1_05 GPIO_EMC_B2_05	O
TXD1	TX_DATA1	ETH3_TX_DATA1	GPIO_EMC_B1_06 GPIO_EMC_B2_06	O
TXD2	TX_DATA2	ETH3_TX_DATA2	GPIO_EMC_B1_01 GPIO_EMC_B2_14	O

Table 42. i.MX RT1180 – ETH3 RGMII pads...*continued*

ETH3		RGMII		
General signal name	MCU signal name	Port	MCU pin	Dir
TXD3	TX_DATA3	ETH3_TX_DATA3	GPIO_EMC_B1_00 GPIO_EMC_B2_13	O
TX_CTL	TX_EN	ETH3_TX_EN	GPIO_EMC_B1_07 GPIO_EMC_B2_07	O
RXC	RX_CLK	ETH3_RX_CLK	GPIO_EMC_B1_02 GPIO_EMC_B2_15	I
RXD0	RX_DATA0	ETH3_RX_DATA0	GPIO_EMC_B1_09 GPIO_EMC_B2_09	I
RXD1	RX_DATA1	ETH3_RX_DATA1	GPIO_EMC_B1_10 GPIO_EMC_B2_10	I
RXD2	RX_DATA2	ETH3_RX_DATA2	GPIO_EMC_B1_04 GPIO_EMC_B2_16	I
RXD3	RX_DATA3	ETH3_RX_DATA3	GPIO_EMC_B1_03 GPIO_EMC_B2_17	I
RX_CTL	RX_EN	ETH3_RX_EN	GPIO_EMC_B1_11 GPIO_EMC_B2_11	I

4.5.8 ETH3 MII/RMII/RGMII pin and clock configuration

According to the required connection (MII/RMII/RGMII), select and configure one of the pins for each signal listed in Table 40 (MII), Table 41 (RMII) or Table 42 (RGMII).

The pin functionality is configured via the `SW_MUX_CTL_PAD_GPIO_n_SW MUX` control register. The pin direction is automatically determined by the selected functionality and it is listed in the column Dir.

Use the settings below for each selected pin and write the settings into the `SW_PAD_CTL_PAD_GPIO_n SW PAD` control register.

- Open Drain – disabled
- PDRV - high drive strength

Output pins (see the Dir column in the tables above):

- Pull Down Pull Up – No Pull

Input pins (see the Dir column in the tables above):

- Pull Down Pull Up – PD

4.5.8.1 MII connection-specific settings

- Set the `MII_PROT` bit in the `NETC_LINK_CFG3` register to 0 (MII).
- The `NETC_CLOCK_ROOT` frequency must be 25 MHz or higher.

4.5.8.2 RMII connection-specific settings

When the RMII connection is used, there are 2 possible ways to generate an RMII reference clock.

1. The RMII reference clock is provided by the MCU (the `ETH3_TX_CLK` port is output).

2. The RMII reference clock is provided by the 50 MHz external oscillator (the ETH3_TX_CLK port is input)

The RMII reference clock is provided by the MCU:

- Set the Sion bit in the SW_MUX_CTL_PAD_GPIO_n_SW MUX control register for the ETH3_TX_CLK pin to 1.
- Set the MII_PROT bit in the NETC_LINK_CFG3 register to 1 (RMII).
- Set the PORT3_RMII_REF_CLK_DIR bit in the NETC_PORT_MISC_CFG register to 1 (the Port3 RMII reference clock is output).
- Use the settings for output pins for ETH3_TX_CLK in the SW_PAD_CTL_PAD_GPIO_n SW PAD control register.
- Enable the SYS_PLL1_DIV2 output (500 MHz). For the correct PLL initialization, read an appropriate chapter in the reference manual.
- Configure the MAC3_CLOCK_ROOT source to 2 (SYS_PLL1_DIV2) and divider to 10. The clock root provides the 50 MHz required by RMII.
- The NETC_CLOCK_ROOT frequency must be 50 MHz or higher.

The RMII reference clock is provided by the 50 MHz external oscillator:

- Use the settings for input pins for ETH3_TX_CLK in the SW_PAD_CTL_PAD_GPIO_n SW PAD control register.
- Set the PORT3_RMII_REF_CLK_DIR bit in the NETC_PORT_MISC_CFG register to 0 (the Port3 RMII reference clock is input).
- The NETC_CLOCK_ROOT frequency must be 50 MHz or higher.

4.5.8.3 RGMII connection-specific settings

- Enable the SYS_PLL1_DIV2 output (500 MHz). For the correct PLL initialization, read an appropriate chapter in the reference manual.
- Configure the MAC3_CLOCK_ROOT source to 2 (SYS_PLL1_DIV2) and divider to 4. The clock root provides the 125 MHz required by RGMII.
- Set the MII_PROT bit in the NETC_LINK_CFG3 register to 2 (RGMII).
- The NETC_CLOCK_ROOT frequency must be 125 MHz or higher.

4.5.9 ETH4 MII, RMII, and RGMII available pins

Table 43. i.MX RT1180 – ETH4 MII pads

ETH4		MII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
TX_CLK	TX_CLK	ETH4_TX_CLK	GPIO_EMC_B1_08 GPIO_EMC_B2_16 GPIO_B1_03	I
TXD0	TX_DATA0	ETH4_TX_DATA0	GPIO_EMC_B1_05 GPIO_EMC_B2_13 GPIO_B1_00	O
TXD1	TX_DATA1	ETH4_TX_DATA1	GPIO_EMC_B1_06 GPIO_EMC_B2_14 GPIO_B1_01	O
TXD2	TX_DATA2	ETH4_TX_DATA2	GPIO_EMC_B1_01 GPIO_EMC_B2_12 GPIO_B1_12	O
TXD3	TX_DATA3	ETH4_TX_DATA3	GPIO_EMC_B1_00 GPIO_EMC_B2_11	O

Table 43. i.MX RT1180 – ETH4 MII pads*...continued*

ETH4		MII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
			GPIO_B1_13	
TX_EN	TX_EN	ETH4_TX_EN	GPIO_EMC_B1_07 GPIO_EMC_B2_15 GPIO_B1_02	O
TX_ER (optional)	TX_ER	ETH4_TX_ER	GPIO_EMC_B1_13 GPIO_EMC_B2_07 GPIO_B1_08	O
RX_CLK	RX_CLK	ETH4_RX_CLK	GPIO_EMC_B1_02 GPIO_EMC_B2_08 GPIO_B1_11	I
RXD0	RX_DATA0	ETH4_RX_DATA0	GPIO_EMC_B1_09 GPIO_EMC_B2_17 GPIO_B1_04	I
RXD1	RX_DATA1	ETH4_RX_DATA1	GPIO_EMC_B1_10 GPIO_EMC_B2_18 GPIO_B1_05	I
RXD2	RX_DATA2	ETH4_RX_DATA2	GPIO_EMC_B1_04 GPIO_EMC_B2_10 GPIO_B1_09	I
RXD3	RX_DATA3	ETH4_RX_DATA3	GPIO_EMC_B1_03 GPIO_EMC_B2_09 GPIO_B1_10	I
RX_DV	RX_EN	ETH4_RX_EN	GPIO_EMC_B1_11 GPIO_EMC_B2_19 GPIO_B1_06	I
RX_ER	RX_ER	ETH4_RX_ER	GPIO_EMC_B1_12 GPIO_EMC_B2_20 GPIO_B1_07	I
CRS	CRS	ETH4_CRS	GPIO_EMC_B1_14 GPIO_EMC_B2_05 GPIO_B2_00	I
COL	COL	ETH4_COL	GPIO_EMC_B1_15 GPIO_EMC_B2_06 GPIO_B2_01	I

Table 44. i.MX RT1180 – ETH4 RMII pads

ETH4		RMII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
REF_CLK	TX_CLK	ETH4_TX_CLK	GPIO_EMC_B1_08 GPIO_EMC_B2_16 GPIO_B1_03	I/O

Table 44. i.MX RT1180 – ETH4 RMII pads*...continued*

ETH4		RMII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
TXD0	TX_DATA0	ETH4_TX_DATA0	GPIO_EMC_B1_05 GPIO_EMC_B2_13 GPIO_B1_00	O
TXD1	TX_DATA1	ETH4_TX_DATA1	GPIO_EMC_B1_06 GPIO_EMC_B2_14 GPIO_B1_01	O
TX_EN	TX_EN	ETH4_TX_EN	GPIO_EMC_B1_07 GPIO_EMC_B2_15 GPIO_B1_02	O
RXD0	RX_DATA0	ETH4_RX_DATA0	GPIO_EMC_B1_09 GPIO_EMC_B2_17 GPIO_B1_04	I
RXD1	RX_DATA1	ETH4_RX_DATA1	GPIO_EMC_B1_10 GPIO_EMC_B2_18 GPIO_B1_05	I
CRS_DV	RX_EN	ETH4_RX_EN	GPIO_EMC_B1_11 GPIO_EMC_B2_19 GPIO_B1_06	I
RX_ER	RX_ER	ETH4_RX_ER	GPIO_EMC_B1_12 GPIO_EMC_B2_20 GPIO_B1_07	I

Table 45. i.MX RT1180 – ETH4 RGMII pads

ETH4		RGMII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
TXC	TX_CLK	ETH4_TX_CLK	GPIO_EMC_B1_08 GPIO_EMC_B2_16 GPIO_B1_03	O
TXD0	TX_DATA0	ETH4_TX_DATA0	GPIO_EMC_B1_05 GPIO_EMC_B2_13 GPIO_B1_00	O
TXD1	TX_DATA1	ETH4_TX_DATA1	GPIO_EMC_B1_06 GPIO_EMC_B2_14 GPIO_B1_01	O
TXD2	TX_DATA2	ETH4_TX_DATA2	GPIO_EMC_B1_01 GPIO_EMC_B2_12 GPIO_B1_12	O
TXD3	TX_DATA3	ETH4_TX_DATA3	GPIO_EMC_B1_00 GPIO_EMC_B2_11 GPIO_B1_13	O
TX_CTL	TX_EN	ETH4_TX_EN	GPIO_EMC_B1_07	O

Table 45. i.MX RT1180 – ETH4 RGMII pads...*continued*

ETH4		RGMII		
General signal name	**MCU signal name**	**Port**	**MCU pin**	**Dir**
			GPIO_EMC_B2_15 GPIO_B1_02	
RXC	RX_CLK	ETH4_RX_CLK	GPIO_EMC_B1_02 GPIO_EMC_B2_08 GPIO_B1_11	I
RXD0	RX_DATA0	ETH4_RX_DATA0	GPIO_EMC_B1_09 GPIO_EMC_B2_17 GPIO_B1_04	I
RXD1	RX_DATA1	ETH4_RX_DATA1	GPIO_EMC_B1_10 GPIO_EMC_B2_18 GPIO_B1_05	I
RXD2	RX_DATA2	ETH4_RX_DATA2	GPIO_EMC_B1_04 GPIO_EMC_B2_10 GPIO_B1_09	I
RXD3	RX_DATA3	ETH4_RX_DATA3	GPIO_EMC_B1_03 GPIO_EMC_B2_09 GPIO_B1_10	I
RX_CTL	RX_EN	ETH4_RX_EN	GPIO_EMC_B1_11 GPIO_EMC_B2_19 GPIO_B1_06	I

4.5.10 ETH4 MII/RMII/RGMII pin and clock configuration

According to the required connection (MII/RMII/RGMII), select and configure one of the pins for each signal listed in Table 43 (MII), Table 44 (RMII) or Table 45 (RGMII).

The pin functionality is configured via the `SW_MUX_CTL_PAD_GPIO_n_SW MUX` control register. The pin direction is automatically determined by the selected functionality and it is listed in the column Dir.

Use the settings below for each selected pin and write the settings into the `SW_PAD_CTL_PAD_GPIO_n SW PAD` control register.

- Open Drain – disabled
- PDRV - high drive strength

Output pins (see the Dir column in the tables above):

- Pull Down Pull Up – No Pull

Input pins (see the Dir column in the tables above):

- Pull Down Pull Up – PD

4.5.10.1 MII connection-specific settings

- Set the `MII_PROT` bit in the `NETC_LINK_CFG4` register to 0 (MII).
- The `NETC_CLOCK_ROOT` frequency must be 25 MHz or higher.

4.5.10.2 RMII connection-specific settings

When the RMII connection is used, there are 2 possible ways to generate an RMII reference clock.

1. The RMII reference clock is provided by the MCU (the ETH4_TX_CLK port is output).
2. The RMII reference clock is provided by the 50 MHz external oscillator (the ETH4_TX_CLK port is input)

The RMII reference clock is provided by the MCU:

- Set the Sion bit in the SW_MUX_CTL_PAD_GPIO_n_SW MUX control register for the ETH4_TX_CLK pin to 1.
- Set the MII_PROT bit in the NETC_LINK_CFG4 register to 1 (RMII).
- Set the PORT4_RMII_REF_CLK_DIR bit in the NETC_PORT_MISC_CFG register to 1 (the Port4 RMII reference clock is output).
- Use the settings for output pins for ETH4_TX_CLK in the SW_PAD_CTL_PAD_GPIO_n SW PAD control register.
- Enable the SYS_PLL1_DIV2 output (500 MHz). For the correct PLL initialization, read an appropriate chapter in the reference manual.
- Configure the MAC4_CLOCK_ROOT source to 2 (SYS_PLL1_DIV2) and divider to 10. The clock root provides the 50 MHz required by RMII.
- The NETC_CLOCK_ROOT frequency must be 50 MHz or higher.

The RMII reference clock is provided by the 50 MHz external oscillator:

- Use the settings for input pins for the ETH4_TX_CLK in SW_PAD_CTL_PAD_GPIO_n SW PAD control register.
- Set the PORT4_RMII_REF_CLK_DIR bit in the NETC_PORT_MISC_CFG register to 0 (the Port4 RMII reference clock is input).
- The NETC_CLOCK_ROOT frequency must be 50 MHz or higher.

4.5.10.3 RGMII connection-specific settings

- Enable the SYS_PLL1_DIV2 output (500 MHz). For the correct PLL initialization, read an appropriate chapter in the reference manual.
- Configure the MAC4_CLOCK_ROOT source to 2 (SYS_PLL1_DIV2) and divider to 4. The clock root provides the 125 MHz required by RGMII.
- Set the MII_PROT bit in the NETC_LINK_CFG4 register to 2 (RGMII).
- The NETC_CLOCK_ROOT frequency must be 125 MHz or higher.

4.5.11 NETC MDIO available pins

Table 46. i.MX RT118x – NETC MDIO pads

NETC		MDIO		
General signal name	**MCU signal name**	**MCU port**	**MCU pin**	**Dir**
MDC	MDC	NETC_MDC	GPIO_EMC_B1_18 GPIO_EMC_B1_40 GPIO_EMC_B2_00 GPIO_EMC_B2_19 GPIO_AD_30 GPIO_SD_B2_11 GPIO_B1_13 GPIO_B2_03	O
MDIO	MDIO	ENET_MDIO_DATA	GPIO_EMC_B1_19 GPIO_EMC_B1_41	I/O

Table 46. i.MX RT118x – NETC MDIO pads*...continued*

NETC		MDIO		
General signal name	**MCU signal name**	**MCU port**	**MCU pin**	**Dir**
			GPIO_EMC_B2_01 GPIO_EMC_B2_20 GPIO_AD_31 GPIO_SD_B2_10 GPIO_B1_12 GPIO_B2_02	

4.5.12 NETC MDIO pin configuration

Use the settings below for `GPIO_EMC_xx, GPIO_SD_xx` and `GPIO_Bx_xx` selected pins and write the settings into the `SW_PAD_CTL_PAD_GPIO_n SW PAD` control register.

- Open Drain – disabled
- PDRV - high drive strength
- Pull Down Pull Up – PD

Use the settings below for `GPIO_AD_xx` pins and write the settings into the `SW_PAD_CTL_PAD_GPIO_n SW PAD` control register.

- Open Drain – disabled
- Pull / Keep Select – Pull Enable
- Pull Up / Down Config - Weak pull down
- Drive Strength - high driver
- Slew Rate - Slow Slew Rate

5 Revision history

Table 47. Revision history

Document ID	Release date	Description
AN14251 v.1.0	20 March 2024	Initial version

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