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Application Note

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Setting the Sample Points for the PowerPC™ MPC7450 L3 Cache

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This application note explains how to set the sample point parameters in the L3 cache control register (L3CR) in the MPC7450 family of microprocessors. While this document refers specifically to the MPC7450, it also applies to any microprocessor based on the MPC7450 that includes a level 3 (L3) interface.

Contents

1 Introduction

The MPC7450 microprocessor implements a flexible, backside L3 cache interface. A critical step in the successful design of a system that implements an L3 cache is the determination of the correct sample points settings to be programmed in the L3CR. Because these settings determine when the processor forwards data from the receive latches of the L3 data signals, incorrect settings may cause unpredictable and non-repeatable results, including data corruption and system instability. Troubleshooting a system in which the sample points have been set incorrectly can be difficult. This document explains how to determine the correct settings and what to do if the settings do not work properly.

When the MPC7450 initiates a read on the L3 interface, it drives the L3 address and control signals based on a clock

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that is phase-aligned with the processor core clock. The processor begins its count of L3 clock and processor clock cycles for the sample point at this time. The L3_CLK*x* signals (and L3_ECHO_CLK[1:3] signals in PB2 and LateWrite modes) are then offset from this clock, such that the L3_CLKs edges are received by the SRAM within the window in which the address and control lines are valid, in order to provide adequate setup and hold times at the SRAM devices; this is shown graphically in Figure 3 and Figure 3. Naturally, there are output driver delays (output valid times) associated with all of the above mentioned signals; these values are provided in the *MPC7450 RISC Microprocessor Hardware Specifications*, and those that impact the sample point settings are further explained in Section 3.2.1, "Processor Delays."

Upon latching the address, the SRAM devices drive the requested data on the L3 data pins some number of L3 clock cycles later; this read latency is determined by the type of SRAM and is discussed in Section 3.1, "SRAM Read Latency." The processor receive latches are synchronized by the L3_ECHO_CLKx signals and data is latched on a rising edge (and falling edge for DDR types) of these signals. When a data beat is latched, it is stored in a receive FIFO so that additional beats can be received even if the processor has not yet sampled the data and forwarded it to the L3 accumulator. There is a delay from the time data is latched on a rising (or falling) echo clock edge to when it is available in the FIFO; this delay is provided in the *MPC7450 RISC Microprocessor Hardware Specifications* and is further explained in Section 3.2.1, "Processor Delays." The data is forwarded from the FIFO to the L3 accumulator when the processor has counted up to the sample point, as determined by the sample point settings in the L3CR.

2 L3 Cache Control Register (L3CR)

Three fields in the L3CR configure the sample point settings. These are described in the following sections.

2.1 L3 Clock Sample Point (L3CKSP)

L3CKSP (L3CR[14:15]) determines how many whole L3_CLKx cycles the processor counts before sampling, providing the coarse granularity in setting the sample points. This value is primarily determined by the read latency of the target SRAM and is measured in L3_CLK cycles. It can also be affected by the hardware latencies in the system should they exceed the maximum setting available in the L3PSP field.

2.2 L3 P-Clock Sample Point (L3PSP)

L3PSP (L3CR[16:18]) determines how many processor clocks (after the expiration of the number of L3 clocks set by L3CKSP) the processor counts before sampling, providing the fine granularity in setting the sample points. It is determined by signal delays on the board and the internal delays of L3_CLKx and L3_ECHO_CLKx. This parameter specifies a particular processor clock edge within an L3 clock, with a zero value corresponding to a processor clock coincident with a rising L3 clock edge so its maximum value is one less than the L3 clock ratio (as set by L3CR[L3CLK]). If a calculated setting for L3PSP exceeds the maximum value, then L3CKSP must be incremented until a valid value of L3PSP is reached. For example, for a system in which the L3 clock ratio is 4:1, the possible values of L3PSP are 0, 1, 2, and 3. If calculations yield a setting of 2 for L3CKSP and 5 for L3PSP, then L3CKSP must be incremented to 3 and L3PSP set to 1.

2.3 L3 Sample Point Override (L3SPO)

Setting the L3SPO bit causes the processor to add one cycle of latency during read operations. The processor reads the programmed L3CR[L3CKSP] value, adds one to it, and samples data at this increased latency. This bit provides forward compatibility with future SRAM devices and should always be cleared for the SRAM types described in this document.

3 Latencies and Delays

The total L3 latency must be calculated from the time when the address is driven on the L3 interface until the data is returned by the SRAM and is valid in the receive FIFO. This latency has two major components:

- SRAM read latency: The amount of time required by the SRAM to return data after latching the address. This information is provided in the SRAM data sheet, and is measured in L3 clock cycles. The following special considerations apply for each type of SRAM:
  - DDR: Data must not be sampled until the second beat of data is valid. In effect, this adds one-half of an L3 clock cycle to the read latency.
  - Pipelined-burst (PB2) and LateWrite: Data must not be sampled until the first beat of data is valid.
- Clock path latency: The total delay associated with the hardware path from the generation of the internal L3_CLKx edge to the reception of the corresponding clock edge at the L3_ECHO_CLKx pins. This has two sub-components:
  - Processor delay: The delays internal to the MPC7450.
  - Hardware delay: All delays external to the processor, including propagation delays on the board, loading delays, and any clocking delays associated with the SRAM (if applicable). These delays are measured in nanoseconds.

3.1 SRAM Read Latency

Each SRAM requires a certain number of clock cycles to access and drive the requested data after latching the address. The SRAM read latency, t_{READ}, is specific to each device and is obtained directly from the SRAM data sheet. The SRAM latency determines the base value for L3CKSP, which then may need to be modified to accommodate the hardware latency. For PB2 and LateWrite SRAM, the data can be sampled after the first beat of data is valid. DDR SRAM requires that sampling not occur until the second beat of data is valid, effectively adding one-half of an L3 clock to the read latency. This is because in DDR mode, the MPC7450 reads two FIFO entries on successive core clocks and returns the two beats to the core simultaneously.

3.2 Clock Path Latency

The clock data latency is the total delay associated with the hardware path of the L3 clock from internal generation to reception as an echo clock. The latency is measured from the time when an internally-generated L3 clock edge (used to drive the L3 address and control pins) occurs to the time the associated echo clock edge is received by the MPC7450. The clock path latency determines L3PSP and may also affect L3CKSP if the calculated value of L3PSP is greater than

the maximum allowed value. The clock path latency is the sum of two component delays, described in the following two sections.

3.2.1 Processor Delays

Processor delays are those delays entirely internal to the MPC7450. These delays must be added to the hardware delays described in Section 3.2.2, "Hardware Delays," to determine the total latency associated with the L3 clock path. Three internal delays must be known:

- t_{AC}: This specification describes a logical offset between the internal clock edge used to drive the L3 address and control signals (this clock edge is phase-aligned with the processor clock edge) and the internal clock edge used to drive the L3_CLKx signals. With proper board routing, this offset ensures that the L3_CLKx edge arrives at the SRAM within a valid address window and provides adequate setup and hold time. This offset is reflected in the L3 bus interface AC timing specifications, but must also be used in the calculation of sample points.
- t_{CO}: This specification is the delay from a rising or falling edge on the internal_L3_CLK signal to the corresponding rising or falling edge at the L3_CLKx pins. This essentially describes an output valid time for the L3_CLKx signals. For PB2 and LateWrite SRAM configurations, this delay also applies to the launch of the clock edge at the L3_ECHO_CLK[1,3] pins. This delay is reflected in the L3 bus interface AC timing specifications, but must also be used in the calculation of sample points.
- t_{ECI}: This specification is the delay from a rising or falling edge of L3_ECHO_CLKx to when data is valid and ready to be sampled from the FIFO. This essentially describes an internal propagation delay from the L3 data pin, through the input buffer, and into the receive FIFO.

The values for these delays are provided in the *MPC7450 RISC Microprocessor Hardware Specifications*.

NOTE

Input setup and hold times for the L3 data signals do not affect the sample point settings.

3.2.2 Hardware Delays

Hardware delays describe the total latencies associated with the physical path of the L3 clock signals. In general, this path is from an L3_CLKx output to an L3_ECHO_CLKx input. Because different types of SRAM use different clocking schemes, the specific nature of this path varies with SRAM type. One example each of MUSG2 DDR and PB2/LateWrite SRAM are given.

4 Sample Point Settings for MSUG2 DDR SRAM

This section provides an example of sample point settings for MSUG2 DDR SRAM. First, all of the delays described in Section 3, "Latencies and Delays," must be determined; then this information is used to determine the earliest sample point. In this example, the following is assumed:

- f_{CORE} = 800 MHz (Q-spec device)
- f_{L3_CLK} = 200 MHz (4:1 core:L3 divider)
- Freescale MCM64E836-4 MUSG2 DDR SRAM

4.1 Calculating the Clock Path Latency

Figure 1 shows the proper signal connections for MSUG2 DDR SRAM.

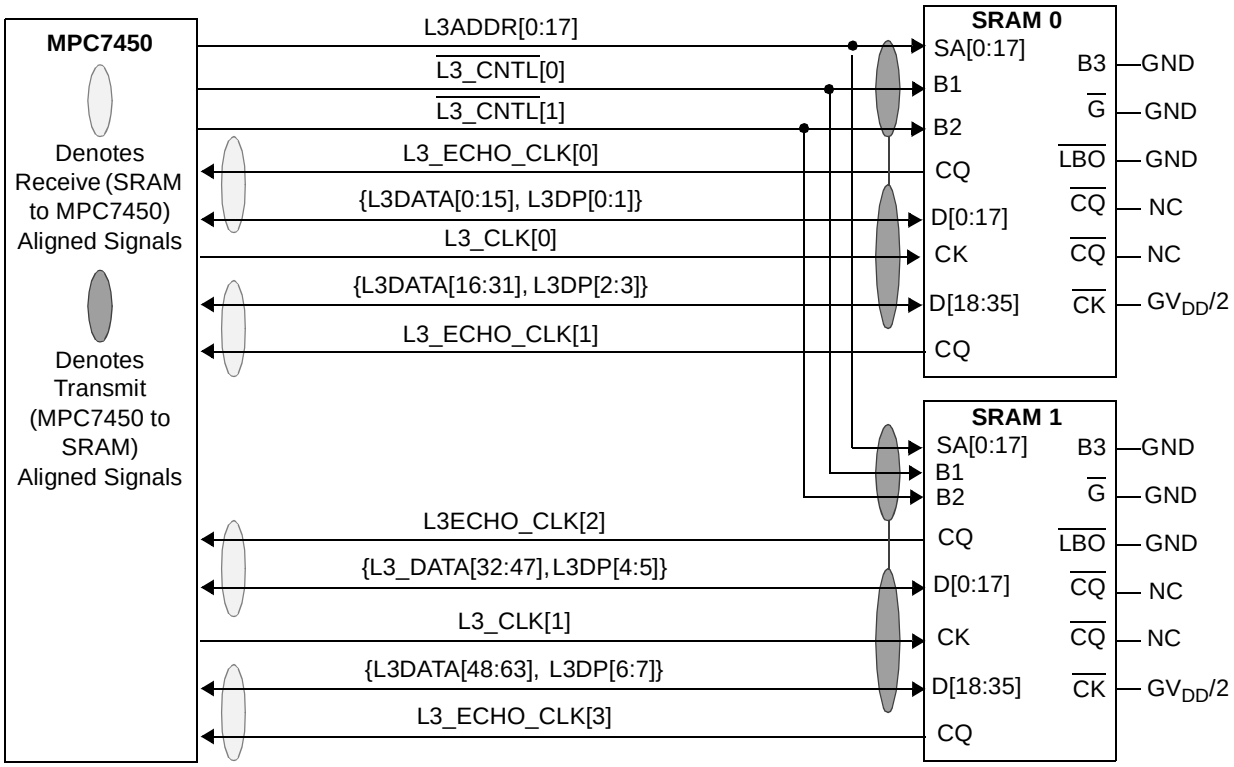


Figure 1. Typical Source-Synchronous 2-Mbyte L3 Cache DDR Interface

Because DDR SRAM devices provide an echo clock, the hardware delay path for this configuration is from the L3_CLKx pin, to the CK pin of the SRAM, through the SRAM to the CQ pin, and back to the L3_ECHO_CLKx pin. This path, with the parameter names of the delays, is shown in Figure 2. The parameter names associated internally with the SRAM, t_{KXCH} and t_{KXCL}, are based on the names given in the data sheet for Freescale's MCM64E836 DDR SRAM. Other manufacturers may use different naming conventions in their data sheets. The greater of these two values should always be used in clock path latency calculations; in this example, because they are equal, either value can be used.

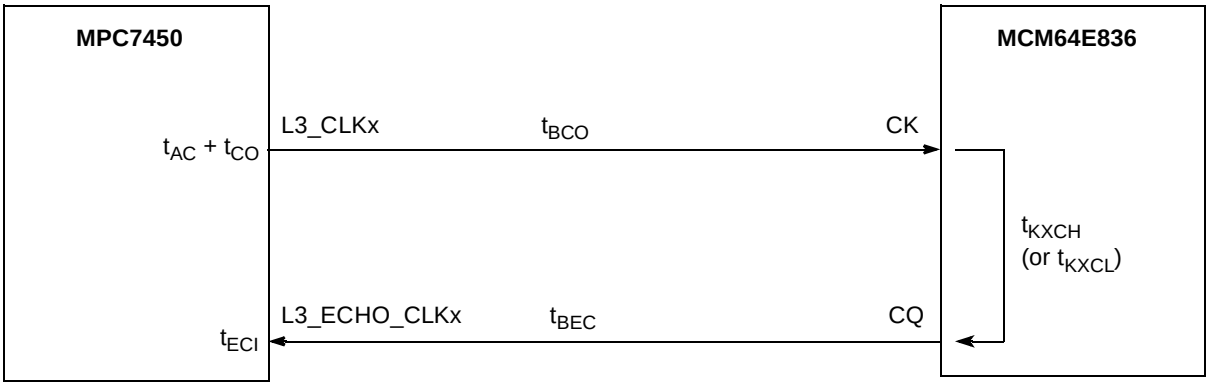


Figure 2. Clock Path for MSUG2 DDR SRAM

The only items in Figure 2 that must be determined by the designer are the board propagation delays, t_{BCO} and t_{BEC}. Because these are entirely system dependent, it is up to the board designer to determine these parameters. This example assumes the following:

- All trace lengths are 2.5 inches
- Unloaded propagation speed on each trace is 180 ps/in.
- Loading delay (as a result of input capacitance) is 10 ps/pF.

Using these approximations, the following equations are used to determine the propagation delays:

$$t_{BCO} = [(\text{trace length}) \times (\text{propagation speed})] + [(\text{SRAM input capacitance}) \times (\text{loading delay})]$$
$$= [(2.5 \text{ in}) \times (180 \text{ ps/in})] + [(6 \text{ pF}) \times (10 \text{ ps/pF})] = 510 \text{ ps} = 0.51 \text{ ns}.$$
$$t_{BEC} = [(\text{trace length}) \times (\text{propagation speed})] + [(\text{L3 input capacitance}) \times (\text{loading delay})]$$
$$= [(2.5 \text{ in}) \times (180 \text{ ps/in})] + [(9.5 \text{ pF}) \times (10 \text{ ps/pF})] = 545 \text{ ps} = 0.55 \text{ ns}.$$

4.2 Calculating the Minimum L3CKSP and L3PSP

Combining the preceding information with the information provided in the SRAM data sheet and *MPC7450 Hardware Specifications*, a table of latencies can be constructed, as shown in Table 1.

Table 1. Latencies for MUSG2 DDR SRAM example

Delay Type	Symbol	Latency	Unit	Data Source
SRAM read latency [1]	t_{READ}	1.5	t_{L3_CLK}	SRAM data sheet
Clock path latency: processor delays	t_{AC}	.75	t_{L3_CLK}	MPC7450 Hardware Specifications
	t_{CO}	3	ns	
	t_{ECI}	3	ns	
clock path latency: hardware delays	t_{BCO}	0.51	ns	Propagation and loading delays (system dependent)
	t_{BEC}	0.55	ns	
	t_{KXCH}	2	ns	SRAM data sheet

[1] This represents the number of L3_CLKx cycles from the time an address is latched by the SRAM to the time when the second beat of data is returned.

The correct values for L3CKSP and L3PSP can now be determined. The total time to the sample point is just the sum of the SRAM read and clock path latencies:

$$t_{SP} = t_{READ} + t_{AC} + t_{CO} + t_{ECI} + t_{BCO} + t_{BEC} + t_{KXCH}$$
$$= (1.5 \times t_{L3\_CLK}) + (0.75 \times t_{L3\_CLK}) + t_{CO} + t_{ECI} + t_{BCO} + t_{BEC} + t_{KXCH} = 20.3 \text{ ns}$$

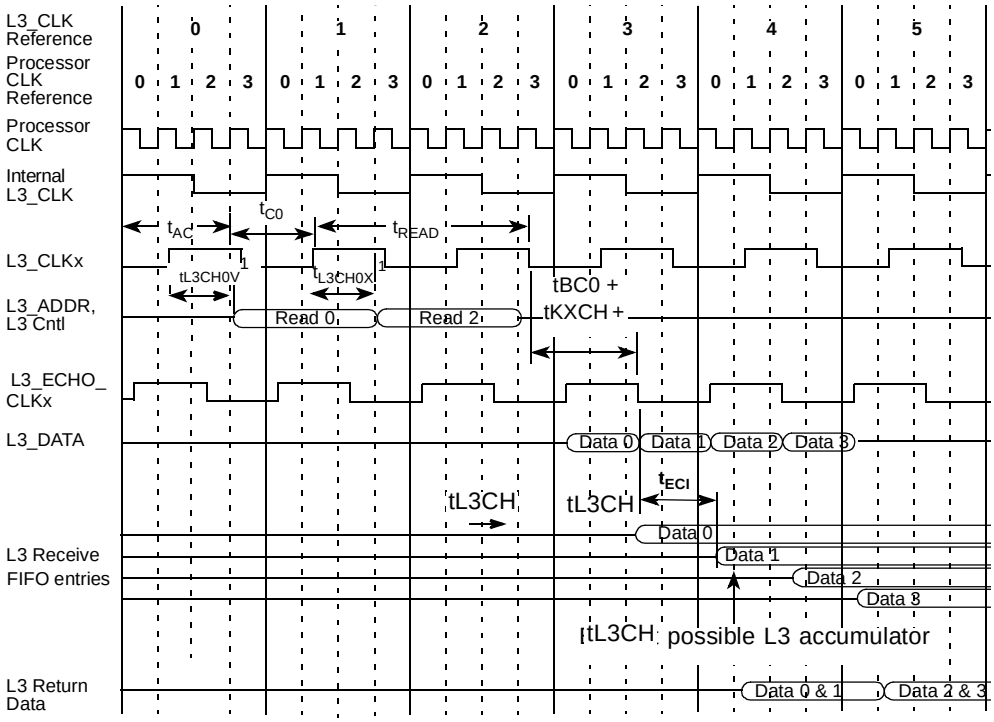
To determine the correct settings, t_{SP} must then be converted into units of L3 clocks and any remainder into processor core clocks. Because each L3 clock has a period of 5 ns and each processor core clock has a period of 1.25 ns, the following conversion is performed:

$$t_{SP} = 20.3 \text{ ns}$$
$$= (4 \times 5 \text{ ns}) + (0 \times 1.25 \text{ ns}) + 0.3 \text{ ns}$$
$$= 4 \text{ L3 clocks} + 0 \text{ core clocks} + 0.3 \text{ ns}$$
$$\approx 4 \text{ L3 clocks} + 1 \text{ core clock}$$

Always round up to the nearest core clock in these calculations because they determine the earliest possible sample point. Because the clock path introduces two L3 clocks of latency, in addition to the 2.5 L3 clocks of the SRAM read latency, L3CKSP must be set to 4. L3PSP is then set to indicate that the processor should sample the data on the first core clock within the fourth L3 clock period. This is shown in Figure 3 and the resulting sample point settings are summarized in Table 2. These settings represent the minimum values for the sample point settings only—more conservative settings are recommended. See Section 6, "Tips and Troubleshooting."

Table 2. Minimum L3CR[L3CKSP] and L3CR[L3PSP] Settings for MSGU2 DDR Example

Parameter	L3CR bits	Value	Setting in L3CR
L3CKSP	L3CR[14–15]	4	0b10
L3PSP	L3CR[16–18]	1	0b001



Notes:

1. t_{L3CHOV} and t_{L3CHOX} are the output valid and output hold times, respectively, for the L3 address and control signals; see the *MPC7450 Hardware Specifications*. They are not used in the calculations to determine the sample point settings and are shown here for reference only.
2. This shows the earliest possible sample point. Sampling should be further delayed by one or more processor core cycles to provide additional assurance data are valid in the FIFO when it is sampled. See Section 6, "Tips and Troubleshooting."

Figure 3. Sample Point Timing Diagram for MUSG2 DDR SRAM Example

5 Sample Point Settings for PB2 and LateWrite SRAM

This section provides an example of sample point settings for PB2 and LateWrite SRAM. First, all of the delays described in Section 3, "Latencies and Delays," must be determined; then this information is used to determine the earliest sample point. In this example, the following are assumed:

- f_{CORE} = 800 MHz (Q-spec part)
- f_{L3_CLK} = 200 MHz (4:1 core:L3 divider)
- Freescale MCM63R836 LateWrite SRAM

Though this example uses LateWrite SRAM, the procedure for determining the sample point settings is identical for PB2 SRAM configurations. Figure 5-1 shows the proper signal connections for LateWrite or PB2 SRAM.

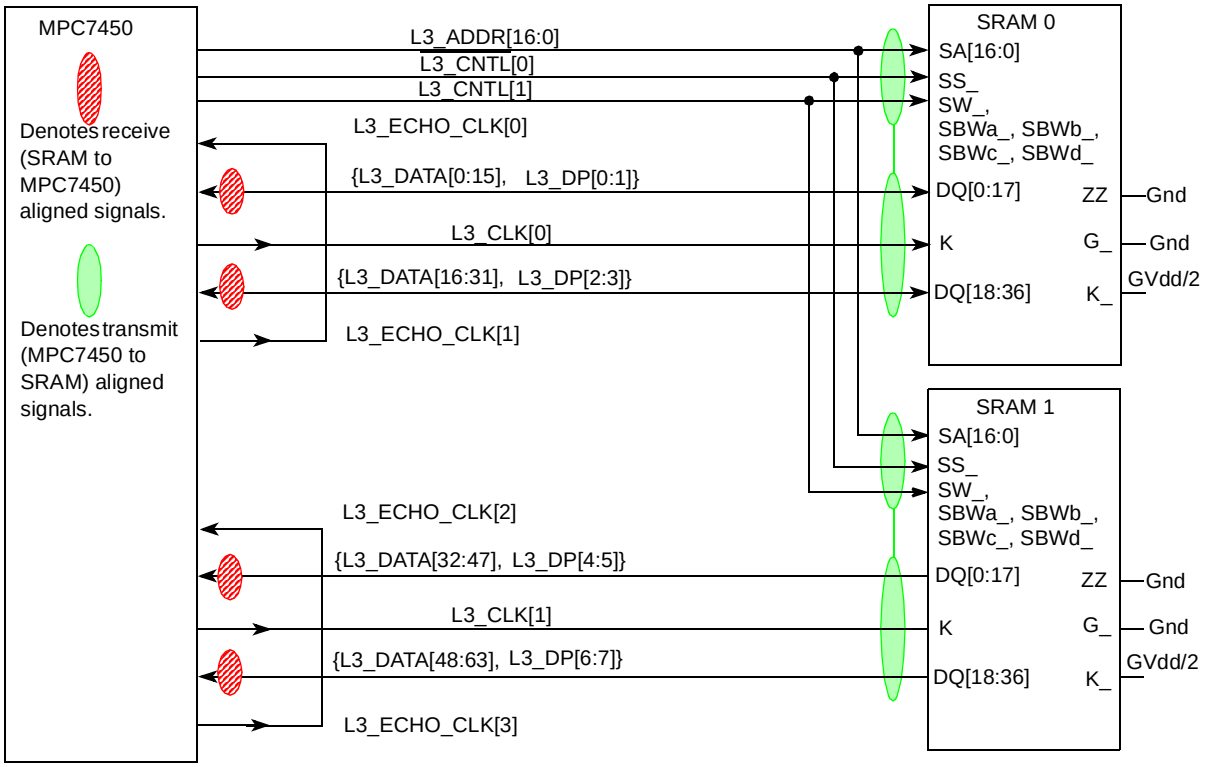


Figure 5-1.Typical Synchronous 1-MByte L3 Cache LateWrite or PB2 Interface

5.1 Calculating the Clock Path Latency

Because PB2 and LateWrite SRAM types do not provides an echo clock, a feedback loop from the L3_ECHO_CLK[1,3], halfway out to the SRAM, and back to L3_ECHO_CLK[0,2] is used instead. This path, with the parameter names of the delays, is shown in Figure 2.

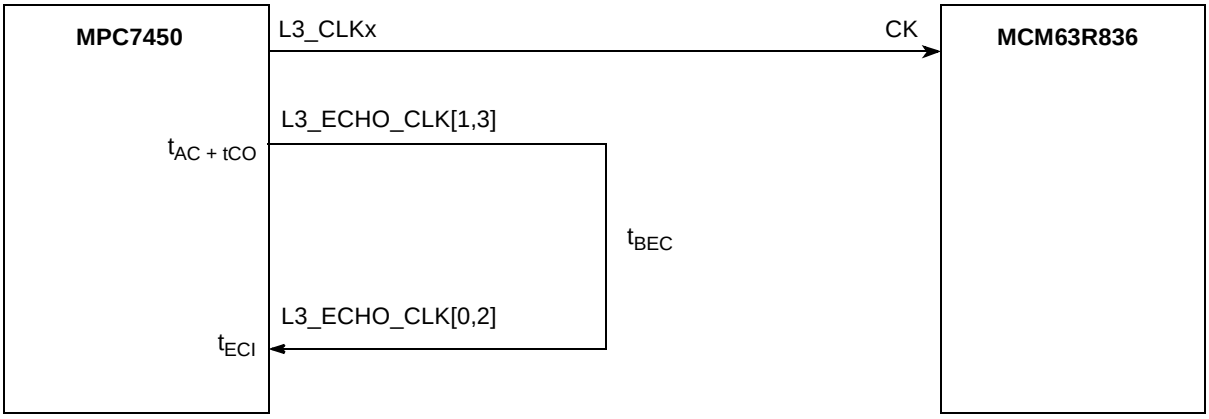


Figure 2. Clock Path for PB2 and LateWrite SRAM

The only item in Figure 2 that must be determined by the designer is the feedback trace propagation delay, t_{BEC}. Because this is entirely system dependent, it is up to the board designer to determine this parameter. This example assumes the following:

- A total feedback loop trace length of 5.0 inches
- Unloaded propagation speed on each trace is 180 ps/in.
- Loading delay (as a result of input capacitance) is 10 ps/pF.

Using these approximations, the following equations are used to determine the propagation delays:

$$t_{BEC} = [(\text{trace length}) \times (\text{propagation speed})] + [(\text{L3 input capacitance}) \times (\text{loading delay})]$$
$$= [(5.0\text{ in}) \times (180\text{ ps/in})] + [(9.5\text{ pF}) \times (10\text{ ps/pF})]$$
$$= 1.0\text{ ns}$$

5.2 Calculating the Minimum L3CKSP and L3PSP

Combining the information above with the information provided in the SRAM data sheet and the *MPC7450 Hardware Specifications*, a table of latencies can be constructed, as shown in Table 5-1.

Table 5-1. Latencies for LateWrite SRAM Example

Delay Type	Symbol	Latency	Unit	Data Source
SRAM Read Latency [1]	**t_{READ}**	**2**	**t_{L3_CLK}**	**SRAM data sheet**
Clock Path Latency: Processor Delays	**t_{AC}**	**.75**	**t_{L3_CLK}**	MPC7450 Hardware Specifications
	t_{CO}	**3**	**ns**	
	t_{ECI}	3	ns	
Clock Path Latency: Hardware Delays	t_{BEC}	1.0	ns	Propagation and loading delays (system dependent)

1 This represents the number of L3_CLKx cycles from the clock edge on which an address is latched by the SRAM to the clock edge on which the first beat of data will be latched by the processor.

Using the information from the previous sections, the correct values for L3CKSP and L3PSP can now be determined. The total time to the sample point is just the sum of the SRAM read and clock path latencies:

$$t_{SP} = t_{READ} + t_{AC} + t_{CO} + t_{ECI} + t_{BEC}$$
$$= (2 \times t_{L3\_CLK}) + (0.75 \times t_{L3\_CLK}) + t_{CO} + t_{ECI} + t_{BEC} = 20.75 \text{ ns}$$

To determine the correct settings, t_{SP} must then be converted into units of L3 clocks and any remainder into processor core clocks. Because each L3 clock has a period of 5 ns and each processor core clock has a period of 1.25 ns, the following conversion is performed:

$$t_{SP} = 20.75 \text{ ns}$$
$$= (4 \times 5 \text{ ns}) + (0 \times 1.25 \text{ ns}) + 0.75 \text{ ns}$$
$$= 4 \text{ L3 clocks} + 0 \text{ core clocks} + 0.75 \text{ ns}$$
$$\approx 4 \text{ L3 clocks} + 1 \text{ core clocks}$$

Note that it is essential to always round up to the nearest core clock in these calculations because they determine the earliest possible sample point. This is shown graphically in Figure 3 and the resulting sample point settings are summarized in Table 2. These settings represent the minimum values for the sample point settings only, and more conservative settings are recommended. For more information, see Section 6, “Tips and Troubleshooting.”

Table 2. Minimum L3CR[L3CKSP] and L3CR[L3PSP] Settings for LateWrite Example

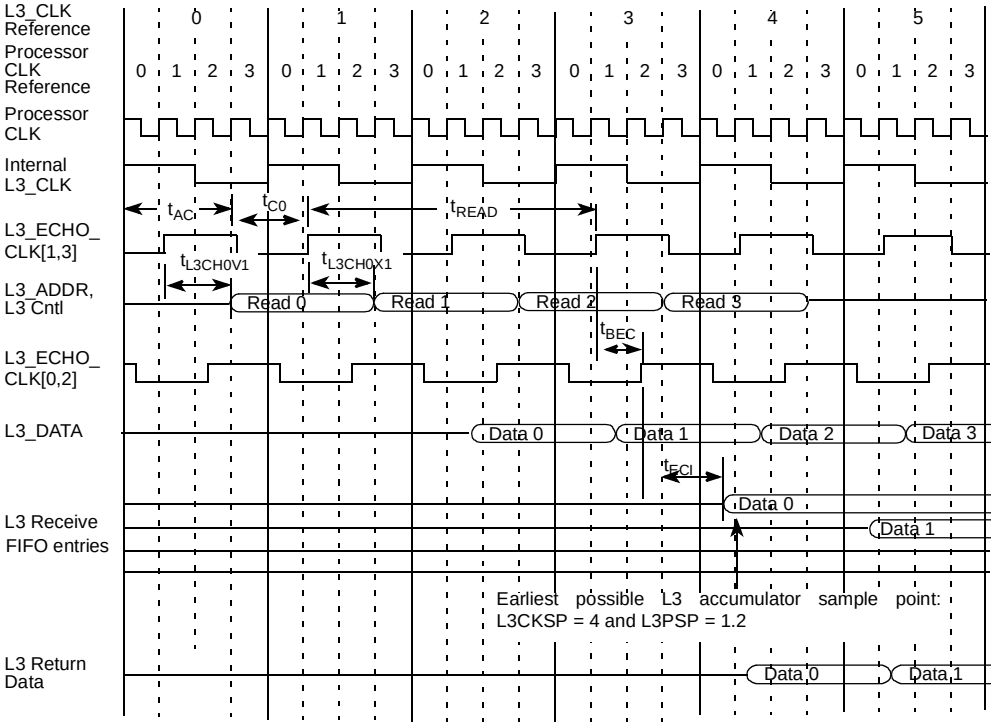
Parameter	L3CR bits	Value	Setting in L3CR
L3CKSP	L3CR[14–15]	4	0b10
L3PSP	L3CR[16–18]	1	0b001

6 Tips and Troubleshooting

The previous examples demonstrate how to determine the minimum sample point settings. One or more extra core clocks can be added in order to provide more guard band. However, because increasing the sample point settings increases the total latency for an L3 load, there is a performance impact associated with doing so. Because of the critical nature of these settings, it is recommended to use the most conservative settings possible while balancing performance considerations. At a minimum, it is recommended that one additional core clock be added to the sample time. In the MSUG2 DDR example, this would yield settings of L3CKSP = 4 and L3PSP = 2; in the LateWrite example, this would yield settings of L3CKSP = 4 and L3PSP = 2.

If these settings are found to be suspect or incorrect, the first step in troubleshooting is to maximize the settings to determine if the problem disappears. (In 4:1 divisor mode, as in the examples, the maximum setting is L3CKSP = 5 and L3PSP = 3.) Note that because a data beat is valid in the FIFO for four L3 clocks and the FIFO can queue up to eight beats of data, there is no concern in a practical system of a FIFO entry becoming invalid or being overwritten as a result of settings that are too high. If the problem disappears when the maximum settings are used, it is likely that incorrect settings had been used previously, and a more thorough investigation of board delays and system latencies is in order; alternatively, trial-and-error can be used to derive sufficient settings. In any event, it is recommended to pad the settings in order to provide a good guard band. If maximizing the settings does not cause the problem to disappear, the settings can be ruled out as the sole cause of the problem and other possible

causes, such as timing violations on the L3 interface, signal integrity issues, or perhaps other incorrect L3 configuration settings, must be investigated.



Notes:

1. t_{L3CHOV} and t_{L3CHOX} are the output valid and output hold times, respectively, for the L3 address and control signals; see the *MPC7450 Hardware Specifications* for more information. They are not used in the calculations to determine the sample point settings and are shown here for reference only.
2. This shows the earliest possible sample point. It is recommended to further delay sampling by one or more processor core cycles to provide additional assurance data will be valid in the FIFO when it is sampled. See Section 6, "Tips and Troubleshooting" for more information.

Figure 3. Sample Point Timing Diagram for LateWrite SRAM Example

7 Document Revision History

Table 3 provides a revision history for this application note.

Table 3. Document Revision History

Rev. No	Substantive Change(s)
0	Initial release.
1	Updated template and corrected numbering system in sections, figures, and tables.
	Changed value of t_{BEC} in Table 3 to 1.0 (typo correction; other instances of t_{BEC} correct)
	Corrected numbering of L3ADDR signals in Figure 1 and Figure 5-1.
	Corrected SRAM read latency in Section 1.5 to 2 and revised Figure 3 correspondingly.
	Nontechnical reformatting

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