



MPC8641D Silicon Changes from Version 2.1 to 3.0

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The Power Architecture™ MPC8641 and MPC8641D version 3.0 silicon incorporates fixes to known errata and improvements to functionality. Some differences described in this document can prevent the MPC8641D version 3.0 silicon from functioning properly. Therefore, this document describes the necessary software changes to accommodate these differences. Block-by-block, it focuses on the changes or enhancements in the device that cause version 3.0 silicon to differ from version 2.1 silicon.

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1 System and Processor Version

Table 1 provides a cross-reference to match the revision level to the processor version register (PVR) and the system version register (SVR). Software that uses the PVR or the SVR must take into account the changes in these values with silicon version 3.0.

Table 1. Revision Level to PVR and SVR Reference

		MPC8641D Rev. 2.1	MPC8641D Rev. 3.0
PVR Value	Single-core MPC8641	0x8004_0202	0x8004_0202
	Dual-core MPC8641D	0x8004_0202	0x8004_0202
SVR Value	Single-core MPC8641	0x8090_0021	0x8090_0030
	Dual-core MPC8641D	0x8090_0121	0x8090_0130

2 e600

This section describes the differences of the e600 interface between silicon version 2.1 and 3.0.

2.1 Fixed MPC8641D Silicon Errata

Table 2 shows the known silicon errata that are fixed in the e600 core interface of the MPC8641D silicon version 3.0.

Table 2. Summary of Fixed DDR MPC8641D Silicon Errata

Number	Title	Disposition
e600 5	Cache failures may occur due to mis-sampled repair fuse information	This erratum is fixed in revision 3.0.

NOTE

The workaround for e600 5 does not need to be implemented for silicon version 3.0. However, if this workaround is applied, silicon version 3.0 continues to work properly.

3 Revision History

Table 3 provides a revision history for this application note.

Table 3. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	07/2009	Initial release.

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