Freescale Semiconductor
Technical Data

MPC7447A Hardware Specification Addendum for the MC7447A*xxnnnn*N*x* Series

This document describes part-number-specific changes to recommended operating conditions and revised electrical specifications, as applicable, from those described in the general *MPC7447A RISC Microprocessor Hardware Specifications*. The MPC7447A is a PowerPC™ microprocessor.

Specifications provided in this document supersede those in the *MPC7447A RISC Microprocessor Hardware Specifications*, Rev. 3 or later, for the part numbers listed in Table 1 only. Specifications not addressed herein are unchanged.

Note that headings and table numbers in this document are not consecutively numbered. They are intended to correspond to the heading or table affected in the general hardware specification.

Part numbers addressed in this document are listed in Table 1.

Freescale Part Numbers Affected:

MC7447AHX600NB
MC7447AHX733NB
MC7447AHX867NB
MC7447AHX1000NB
MC7447AHX1167NB
MC7447AVS600NB
MC7447AVS733NB
MC7447AVS867NB
MC7447AVS1000NB
MC7447AVS1167NB

MC7447AVU600NB
MC7447AVU733NB
MC7447AVU867NB
MC7447AVU1000NB
MC7447AVU1167NB

Table 1. Part Numbers Addressed by this Data Sheet

Freescale Part Number	Operating Conditions			Significant Differences from Hardware Specification
	CPU Frequency (MHz)	V_{DD}	T_j (°C)	
MC7447AHX600NB	600	1.1 V ± 50 mV	0 to 105	Modified core frequency and voltage to reduce power consumption.
MC7447AHX733NB	733			
MC7447AHX867NB	867			
MC7447AHX1000NB	1000			
MC7447AHX1167NB	1167			
MC7447AVS600NB	600			
MC7447AVS733NB	733			
MC7447AVS867NB	867			
MC7447AVS1000NB	1000			
MC7447AVS1167NB	1167			
MC7447AVU600NB	600			
MC7447AVU733NB	733			
MC7447AVU867NB	867			
MC7447AVU1000NB	1000			
MC7447AVU1167NB	1167			

1 General Parameters

Core power supply   1.1 V ± 50 mV DC (nominal), or

1.0 V ± 50 mV DC (derated)

1.1 DC Electrical Characteristics

Table 2 provides the recommended operating conditions for the MPC7447A part numbers described herein.

NOTE

Table 2 describes the nominal operating conditions of the device. For information regarding the operation of the device at supported derated core voltage conditions, see Section 1.3, "Voltage and Frequency Derating."

Table 2. Recommended Operating Conditions [1]

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.1 V ± 50 mV	V	3
PLL supply voltage	AV_{DD}	1.1 V ± 50 mV	V	2, 3

Note:

1. These are the recommended and tested operating conditions. In addition, these devices also support voltage derating; see Section 1.3, "Voltage and Frequency Derating." Proper device operation outside of these conditions and those specified in Section 1.3 is not guaranteed.

2. This voltage is the input to the filter discussed in *MPC7447A RISC Microprocessor Hardware Specifications*, Section 9.2, "PLL Power Supply Filtering," and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.

3. V_{DD} and AV_{DD} may be reduced in order to reduce power consumption if further maximum core frequency constraints are observed. See Section 1.3, "Voltage and Frequency Derating," for specific information.

Table 3 provides the power consumption for the MPC7447A part numbers described herein. For information regarding power consumption when dynamic frequency switching (DFS) is enabled, see the *MPC7447A RISC Microprocessor Hardware Specifications*.

NOTE

The power consumption information in this table applies when the device is operated at the nominal core voltage indicated in Table 2. For power consumption at derated core voltage conditions, see Section 1.3, "Voltage and Frequency Derating."

Table 3. Power Consumption for MPC7447A

	Processor (CPU) Frequency					Unit	Notes
	600 MHz	733 MHz	867 MHz	1000 MHz	1167 MHz		
Full-Power Mode							
Typical	6.0	6.8	7.8	8.0	9.2	W	1, 2
Maximum	8.2	9.5	10.3	11.5	13.0	W	1, 3
Nap Mode							
Typical	1.3	1.3	1.3	1.3	1.3	W	1, 2
Sleep Mode							
Typical	1.3	1.3	1.3	1.3	1.3	W	1, 2

Table 3. Power Consumption for MPC7447A (continued)

	Processor (CPU) Frequency					Unit	Notes
	600 MHz	**733 MHz**	**867 MHz**	**1000 MHz**	**1167 MHz**		
Deep Sleep Mode (PLL Disabled)							
Typical	1.2	1.2	1.2	1.2	1.2	W	1, 2

Notes:

1. These values apply for all valid processor buses. The values do not include I/O supply power (OV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} power is system dependent but is typically < 5% of V_{DD} power. Worst case power consumption for AV_{DD} < 3 mW.

2. Typical power is an average value measured at the nominal recommended V_{DD} (see Table 2) and 65°C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz.

3. Maximum power is the average measured at nominal V_{DD} and maximum operating junction temperature (see Table 2) while running an entirely cache-resident, contrived sequence of instructions which keep all the execution units maximally busy.

4. Doze mode is not a user-definable state; it is an intermediate state between full-power and either nap or sleep mode. As a result, power consumption for this mode is not tested.

1.2 AC Electrical Characteristics

Table 4 provides the clock AC timing specifications for the MPC7447A part numbers described herein.

NOTE

The core frequency information in this table applies when the device is operated at the nominal core voltage indicated in Table 2. For core frequency specifications at derated core voltage conditions, see Section 1.3, "Voltage and Frequency Derating."

Table 4. Clock AC Timing Specifications

At recommended operating conditions. See Table 2.

Characteristic	Symbol	Maximum Processor Core Frequency										Unit	Notes
		600 MHz		**733 MHz**		**867 MHz**		**1000 MHz**		**1167 MHz**			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Processor frequency	f_{core}	500	600	500	733	500	867	500	1000	500	1167	MHz	1, 2, 3
VCO frequency	f_{VCO}	1000	1200	1000	1466	1000	1733	1000	2000	1000	2333	MHz	1, 3

Notes:

1. **Caution**: The SYSCLK frequency and PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in *MPC7447A RISC Microprocessor Hardware Specifications,* Section 9.1, "PLL Configuration," for valid PLL_CFG[0:4] settings.

2. **Caution**: If dynamic frequency switching (DFS) is enabled, the SYSCLK frequency and PLL_CFG[0:4] settings must be chosen such that the resulting processor frequency is greater than or equal to the minimum core frequency.

3. **Caution**: These values specify the maximum processor core and VCO frequencies when the device is operated at the nominal core voltage. If operating the device at the derated core voltage, the processor core and VCO frequencies must be reduced. See Section 1.3, "Voltage and Frequency Derating," for more information.

1.2.1 Processor Bus AC Specifications

Devices described by this hardware specification addendum conform to the processor bus AC timing specifications provided in the *MPC7447A RISC Microprocessor Hardware Specifications*. Please refer to that document for this information.

1.3 Voltage and Frequency Derating

To reduce the power consumption of the device, these devices support voltage and frequency derating whereby the core voltage (V_{DD}) may be reduced if the reduced maximum processor core frequency requirements are observed. The supported derated core voltage, resulting maximum processor core frequency (f_{core}), and power consumption are provided in Table 5. Only those parameters in Table 5 are affected; all other parameter specifications are unaffected.

Table 5. Supported Voltage, Core Frequency, and Power Consumption Derating

Maximum Rated Core Frequency (Device Marking)	Supported Derated Core Voltage (V_{DD})	Maximum Derated Core Frequency (f_{core})	Full-Power Mode Power Consumption	
			Maximum	**Typical**
600	1.0 V ±50mV	533	5.9 W	4.2 W
733		533	5.9 W	4.2 W
867		667	6.9 W	4.9 W
1000		800	8.0 W	5.6 W
1167		1000	9.4 W	6.6 W

2 Ordering Information

2.1 Part Numbers Addressed by This Specification

Table 6 provides the ordering information for the MPC7447A parts described in this document.

Table 6. Part Marking Nomenclature

MC	7447A	*xx*	nnnn	*N*	*x*
Product Code	**Part Identifier**	**Package**	**Processor Frequency** [1]	**Application Modifier**	**Revision Level**
MC	7447A	HX = HCTE BGA VS = RoHS LGA VU = RoHS BGA	600 733 867 1000 1167	N: 1.1 V ± 50 mV 0 to 105°C	B:1.1:PVR = 8003 0101

Notes:

1. Processor core frequencies supported by parts addressed by this specification only. Parts addressed by other specifications may support other maximum core frequencies.

2.2 Part Marking

Parts are marked as the example shown in Figure 1.


```
            MC7447A
            xxnnnnNB

            AWLYYWW
            MMMMMM
            YWWLAZ


             7447A
            BGA/LGA
```
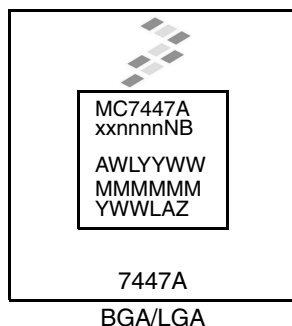
Notes:
  AWLYYWW is the test code.
  MMMMMM is the M00 (mask) number.
  YWWLAZ is the assembly traceability code.

Figure 1. Part Marking for BGA Device

3 Document Revision History

Table 7 provides a revision history for this part number specification.

Table 7. . Document Revision History

Rev. No.	Date	Substantive Change(s)
3	09/23/05	Added RoHS BGA parts: • MC7447AVU600NB • MC7447AVU733NB • MC7447AVU867NB • MC7447AVU1000NB • MC7447AVU1167NB
2	01/24/05	Added LGA parts: • MC7447AVS600NB • MC7447AVS733NB • MC7447AVS867NB • MC7447AVS1000NB • MC7447AVS1167NB
1	09/20/04	Changed title wording from 'Part Number Specification' to 'Hardware Specification Addendum'; adopted new Document ID numbering scheme.
	09/09/04	Added information on derating.
	08/27/04	Added 600-, 733- and 867-MHz speed bins.
0		Initial release.

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