



# Errata to MPC750 RISC Microprocessor Family User's Manual, Rev. 1

This errata describes corrections to the *MPC750 RISC Microprocessor User's Manual*, Revision 1. For convenience, the section number and page number of the errata item in the reference manual are provided. Items in bold are new since the last revision of this document.

To locate any published updates for this document, visit our website listed on the back cover of this document.

**C.4.2.2, C-16** In Section C.4.2.2, “isync Instruction Use with mtsr, mtsrin, and mtmsr” update the paragraph as follows:

The MPC750 and MPC755 have a restriction on the use of the **mtsr**, **mtsrin** or **mtmsr** instructions not described in the *Programming Environments Manual* or in Chapter 2, “Programming Model.” The MPC750 and MPC755 require that an **isync** instruction be executed after either an **mtsr** or **mtsrin** or **mtmsr** instruction. This **isync** instruction must occur after the execution of the **mtsr** or **mtsrin** or **mtmsr** and before the data address translation mechanism uses any of the on-chip segment registers.

**C.5.2.3.2, C-24** In Section C.5.2.3.2, “Address Translation for Data Cache Locking,” update the code at the end of the section as follows:

```
# Enable instruction and data memory address translation. This
# corresponds to setting IR and DR in the MSR (bits 26 & 27)

mfmsr    r1
ori      r1, r1, 0x0030
sync
mtmsr    r1
isync
```

**C.5.2.3.3, C-25** In Section C.5.2.3.3, “Disabling Exceptions for Data Cache Locking,” update the code at the end of the section as follows:

```
# Clear the following bits from the MSR:
#   EE (16)      ME (19)
#   FE0 (20)    FE1 (23)

mfmsr    r1
lis      r2, 0xFFFF
ori      r2, r2, 0x66FF
and      r1, r1, r2
sync
mtmsr    r1
isync
```

**C.5.2.3.10, C-30** In Section C.5.2.3.10, “Address Translation for Instruction Cache Locking,” update the code at the end of the section as follows:

```
# Enable instruction and data memory address translation. This
# corresponds to setting IR and DR in the MSR (bits 26 & 27)

mfmsr    r1
ori      r1, r1, 0x0030
sync
mtmsr    r1
isync
```

**C.5.2.3.11, C-30** In Section C.5.2.3.11, “Disabling Exceptions for Instruction Cache Locking,” update the code at the end of the section as follows:

```
# Clear the following bits from the MSR:
#   EE (16)      ME (19)
#   FE0 (20)    FE1 (23)

mfmsr    r1
lis      r2, 0xFFFF
ori      r2, r2, 0x66FF
and      r1, r1, r2
sync
mtmsr    r1
isync
```

**C.11.6.2, C-72** Add sentence “The L2 tags must be globally invalidated before the L2 is enabled as a cache, private memory, or shared cache and private memory.”



**How to Reach Us:**

**Home Page:**  
[freescale.com](http://freescale.com)

**Web Support:**  
[freescale.com/support](http://freescale.com/support)

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: [freescale.com/SalesTermsandConditions](http://freescale.com/SalesTermsandConditions).

Freescale, and the Freescale logo are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. All other product or service names are the property of their respective owners. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

© 2007, 2014 Freescale Semiconductor, Inc.

Document Number: MPC750UMAD  
Rev. 1.2  
03/2014

