Thermal Management of a C4/Ceramic-Ball-Grid Array: The Motorola PowerPC 603™ and PowerPC 604™ RISC Microprocessors

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ABSTRACT

This paper presents various thermal management options available for controlled-collapse-chip-connection (C4) die attached to a ceramic-ball-grid-array substrate (CBGA), as they apply to low-end/midrange computer products. Computational - fluid-dynamics (CFD) methods are used to solve the conjugate heat transfer problems. CFD modeling is used to predict die-junction temperatures for the PowerPC 603 and PowerPC 604 microprocessor in a single-chip C4/CBGA package. The focus is the die temperature rise for a limited range of boundary conditions, including: substrate conductivity, heat sinks and heat sink attach. For the PowerPC 604 microprocessor die-junction temperature rise is presented for convective air cooling (to 4 m/s) using several commercially-available heat sinks.

NOMENCLATURE

Q_c = die power, W

Θ_{jc} = die junction-to-case resistance, °C/W

Θ_{jl} = die junction-to-lead (i.e., ball) resistance, °C/W

Θ_{ja} = die junction-to-ambient resistance, °C/W

T_j = die junction temperature, °C

T_a = ambient (inlet) temperature of cooling fluid, °C

T_c = package case temperature, °C

T_l = package lead temperature, °C.

INTRODUCTION

PowerPC 603 and PowerPC 604 RISC Microprocessors

The scaleable PowerPC™ microprocessor family (Figure 1), jointly developed by Apple, IBM, and Motorola, is being designed into high-performance cost-effective computers (including notebooks, desktops, workstations, and servers). The PowerPC microprocessor family ranges from the PowerPC 601™ microprocessor to the PowerPC 620™ microprocessor. The PowerPC 603 microprocessor is a low-power implementation of the PowerPC Reduced-Instruction-Set-Computer (RISC) architecture. The PowerPC 604 microprocessor is a 32-bit implementation of the PowerPC architecture, and is software and bus compatible with the PowerPC 601 and PowerPC 603 microprocessors. Both the Motorola PowerPC 603 and PowerPC 604 microprocessors are available in the 21mm controlled-collapsed-chip-connection/ceramic-ball-grid-array single-chip package (C4/CBGA) (Figure 2) [1,2].

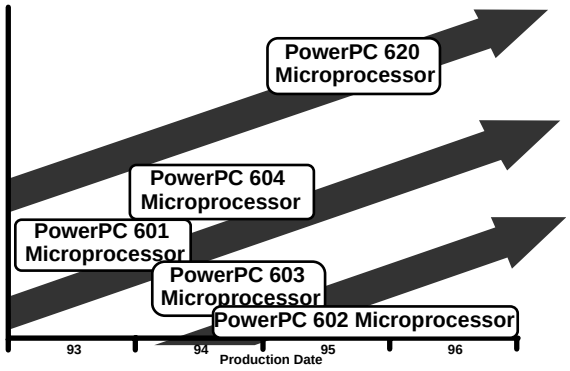

Figure 1. The PowerPC Microprocessor Family.

Objective

This paper presents the thermal management options for the first two C4/CBGA PowerPC RISC microprocessors that have been introduced by Motorola; that is, the PowerPC 603 and PowerPC 604 microprocessor in a 21mm CBGA. We will examine thermal control techniques for an air-cooled C4/CBGA technology, applicable from low-end to midrange computer systems (e.g., personal computers, workstations, file servers, and minicomputers). That is, we will investigate the effect of: component board population, heat sinking, and airflow velocity has on the die-junction temperature.

BACKGROUND

Recent Semiconductor Trends

Computer system performance has dramatically improved over the past three decades. Much of this improvement is a result of increased integration of components at the semiconductor level, made possible by reduced feature sizes. These reduced feature sizes have resulted in several semiconductor integrated-circuit (IC) trends, all of which are increasing: gate count, chip inputs/outputs, chip size, operating frequency, and power consumption. These trends have placed an increased emphasis on microelectronics packaging design.

C4-Ceramic-Ball-Grid Array Package

The use of C4 die on a CBGA interconnect technology offers significant reduction in both the signal delay and the microelectronic packaging volume [3-8]. Figure 2 shows the salient features of the C4/CBGA interconnect technology with an optional heat sink. The C4 interconnection provides both the electrical and the mechanical connections for the die to the ceramic substrate. After the C4 solder bump is reflowed, epoxy (encapsulant) is under-filled between the die and the substrate. Under-fill material is commonly used on large high-power die; however, this is not a requirement of the C4 technology. An alternate implementation of C4/CBGA technology incorporates an aluminum cap with thermal paste internally sealed [3]. The package substrate is a 21mm multilayer-cofired ceramic. The package-to-board interconnection is by an array of orthogonal 90/10 (lead/tin) solder balls on 1.27 mm pitch. During assembly of the C4/CBGA package to the board, the high-melt balls do not collapse [4].

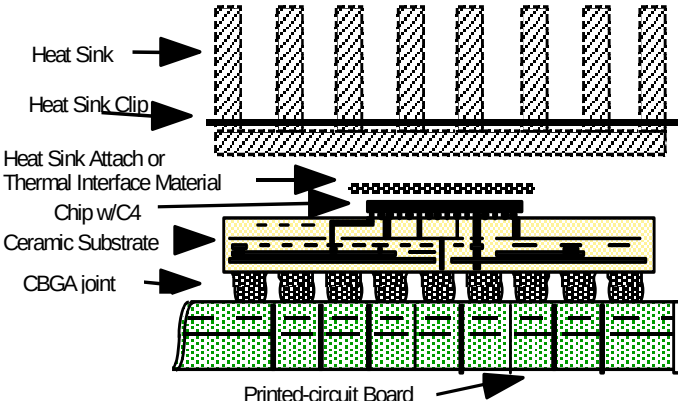

Figure 2. C4 Ceramic-Ball-Grid Array: Exploded Cross-sectional View with Optional Heat Sink (not to scale).

C4/CBGA requires less board routing space than a C4 ceramic-quad-flat package (C4/CQFP). Furthermore, the C4/CQFP gull-wing leads require additional board area for wiring fan-out for electrical routing. Therefore, the C4/CBGA offers the same connections in a significantly smaller board area than a comparable C4/CQFP (Figure 3). However, this area reduction

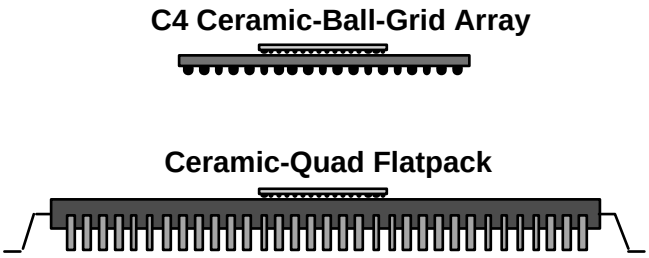

Figure 3. Size Comparison: 21 mm C4-Ceramic-ball-grid array versus a 40 mm Ceramic-quad-flat package (approximate scale and similar lead count) .

results in an approximate four-fold increase in package-level thermal flux density.

For most single-chip packaging technologies the method of connection for the power, ground, and signals to the next-level interconnect (e.g. printed-circuit board, PCB) often presents another challenge for adequate heat removal. That is, a conflict often exists between needs for electrical interconnect and the needs to design an adequate heat conduction path to minimize the package thermal resistance. However, the C4/CBGA technology is unique in that it allows electrical interconnect on the ball-array side, while allowing the back of the die exposed for thermal management options. Thermal control of these microelectronic devices is required for proper operation and acceptable reliability.

Traditional Thermal Package Metrics

Common figures-of-merit used for the comparison of various thermal control designs of microelectronic packaging technologies are the die junction-to-ambient, die junction-to-case, and die junction-to-lead thermal resistance:

$$\Theta_{ja} = (T_j - T_a)/Q_c \quad (1)$$

$$\Theta jc = (Tj - Tc)/Qc \quad (2)$$

$$\Theta jl = (Tj - Tl)/Qc \quad (3)$$

These metrics are often misleading as no single parameter can adequately describe three-dimensional heat flow, which is a function of many parameters, such as: geometry, heat source and placement, package orientation, next-level package attachment, heat sink efficiency and method of chip connection. Many references in the literature discuss both the use and the limitations of these metrics [9,10,11]. In contrast for this paper, the die-junction component temperature rise above ambient for the stated power dissipation and its boundary conditions will be presented. However, these particular results are only applicable to the C4/CBGA single-chip package for the assumptions outlined in this study.

C4/CBGA HEAT TRANSFER PATHS

Attached Heat Sink: Primary Heat Transfer Path

To increase the thermal dissipation capability of this technology, a heat sink may be mated to the silicon (i.e., the package case). A variety of commercially-available active and passive heat sinks products are presently available [14]. Heatsinks considered in

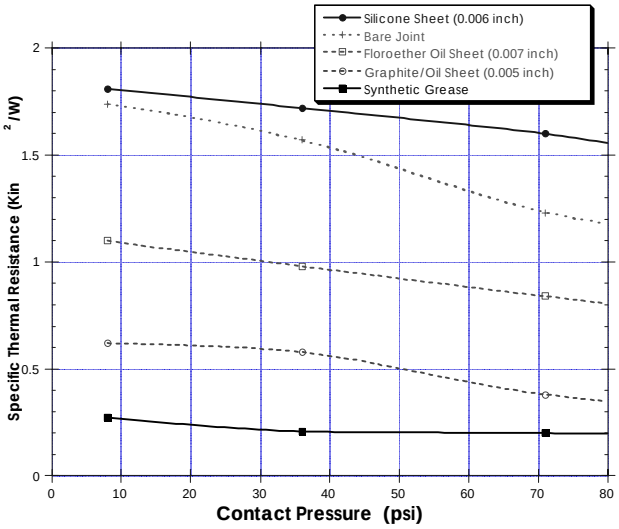

Figure 4. Thermal Performance of Select Thermal Interface Material (adapted from [15])

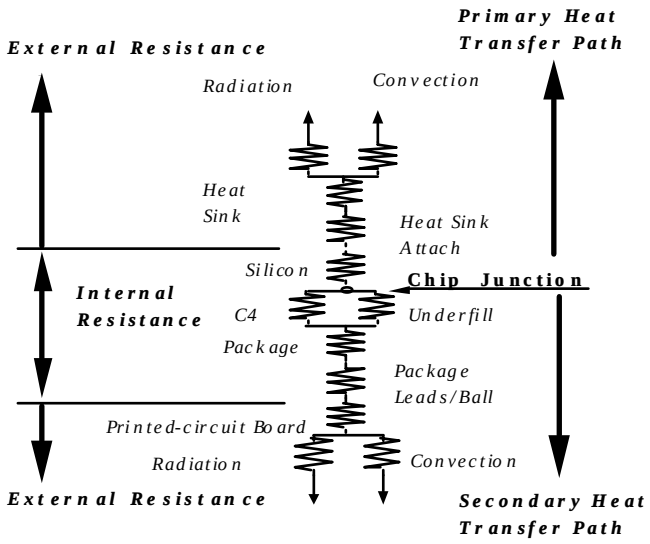

Figure 5. Simplified Thermal Network: a C4-Ceramic-Ball-Grid-Array Package mounted to a Printed-circuit Board. (Note, the internal versus external package resistance.)

this study included: 1) several pin-fins, 2) bi-directional, 3) stamped, and 4) a pin-fin heat sink with an attached cooling fan (Table 1, Appendix). The integral fan heat sink, promotes local impingement airflow, at a approximate 1 watt power draw. These fans are typically offered in 5 and 12 volt DC brushless motors. The heat sinks for this study, were chosen for their power dissipation range for low-airflow velocities and geometric compatibility with the 21 mm ceramic body.

Due to silicon die fragility, any heat sink attach scheme must take into consideration structural compliance to avoid damage to the die. In addition, for those applications where the heat sink is attached by spring force or threaded, a thermal interface material may be used at the die-to-heat sink interface to minimize the thermal contact resistance. Figure 4 shows the thermal performance of three thin sheet interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure [15]. These thermal interface materials performance improve with increasing contact pressure. The use of thermal grease and the graphite-oil sheet significantly reduce the interface resistance. That is, the bare joint results in a thermal resistance approximately 7 times greater than the thermal grease joint. For nominally flat surfaces that are brought into intimate contact, as in the case of the bare joint and joint with thermal grease, the thermal performance is a function of: contact pressure, surface finish, material hardness and interstitial fluid conductivity. The data presented in Figure 4 is for aluminum/aluminum interfaces that were 2.54 cm cross-sectional area; however, these results may be used as a guide to show the improvement thermal interface materials offer over bare joints [15]. Of course the selection of any thermal interface material depends on many factors, such as: thermal performance requirements, manufacturability, service temperature, dielectric properties and cost.

Several heat sink attach options exist: 1) Two mechanical integral spring-clip styles attach to through-holes in the printed-circuit board. One implementation is the use of a torsion "Z-spring" that clips under J-clips (2 each) soldered in the printed-circuit board; while, the other beam springs clips to four through-holes in the printed-circuit board. 2) For the CBGA package a female threaded connector clips to the package body, then the heat sink containing a male thread is tightened to make contact with the die. 3) The use of low-shear stress adhesives might be applicable for low mass heat sinks in benign shock and vibration environments.

For cases with an attached heat sink, the primary heat transfer path is as follows (Figure 5). Heat generated on the active side (ball) of the chip is conducted through the silicon, then through the heat sink attach material and finally to the heat sink where it is removed by natural or forced-air convection.

For a one-dimensional adiabatic-board case, the die junction-to-case resistance may be expressed as,

$$\Theta = \Theta_{\text{silicon}} \qquad (4)$$

Then the junction-to-ambient resistance is,

$$\Theta = \Theta_{jc} + \Theta_{\text{heat sink attach}} + \Theta_{\text{heat sink}} \qquad (5)$$

The silicon thermal resistance is quite small, therefore; for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material (or thermal interface material) and the heat sink conduction/convective thermal resistances are the dominant terms.

Alternate Heat Transfer Path

For lower-power microprocessors, the use of a heat sink may not be necessary. Heat conducted through the silicon may be convectively removed to the ambient air. In addition a second

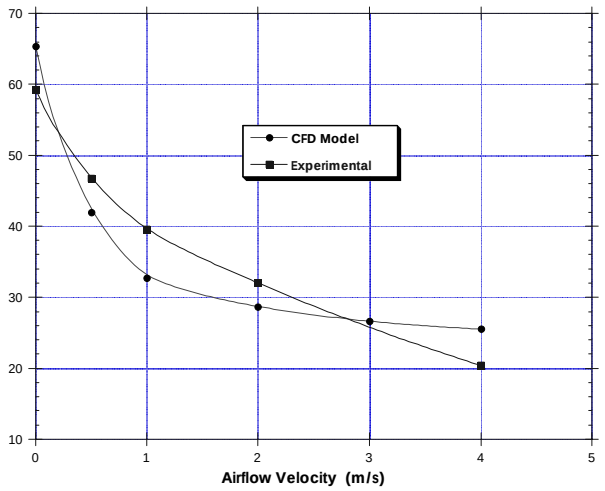

Figure 6. CFD Model Results versus Experimental Data (3 watt, no heat sink).

parallel heat flow path exists by conduction, through the C4 bumps and the epoxy under-fill, to the ceramic substrate for further convection cooling off the edges (Figure 5). Then from the ceramic substrate heat is conducted via the leads/balls to the next-level interconnect; whereupon the primary mode of heat transfer is by convection and/or radiation. This path alone may be adequate for low-power chips, however, it is a function of the board population and the system-level boundary conditions.

The internal-package conduction resistance terms for the secondary heat transfer path is the contribution of: C4, under-fill, package substrate, package leads/balls. For a one-dimensional model, the die junction-to-lead thermal resistance is:

$$\Theta_{jl} = 1/(1/\Theta_{c4} + 1/\Theta_{\text{under-fill}}) + \Theta_{\text{package}} + \Theta_{\text{lead}} \quad (6)$$

Experimental Program

A CBGA with a C4 thermal test die was utilized for package thermal characterization. To sense temperature, the die contained four resistance-thermal devices (RTD) in various locations on the chip. This temperature transducer required calibration prior to use. For all the thermal test vehicles, the RTD for die-junction temperature measurements were calibrated in a forced-convection oven. The oven temperature was stepped over the range of 25°C to 110°C. The calibration data is accurately described by a linear correlation over the range of interest. A low-velocity wind tunnel with a 30.5 cm-square-test section was used for all forced-air cooling studies. Free-stream air velocities were measured using a hot-wire anemometer system. The C4/CBGA printed-circuit-board test vehicle was placed in the center of the test sections [12].

RESULTS AND DISCUSSION

Computational Fluid Dynamics Models

Computational fluid dynamics (CFD) methods were used to solve the steady-state conjugate heat transfer problem using a commercial finite-volume method [13]. The calculation domain

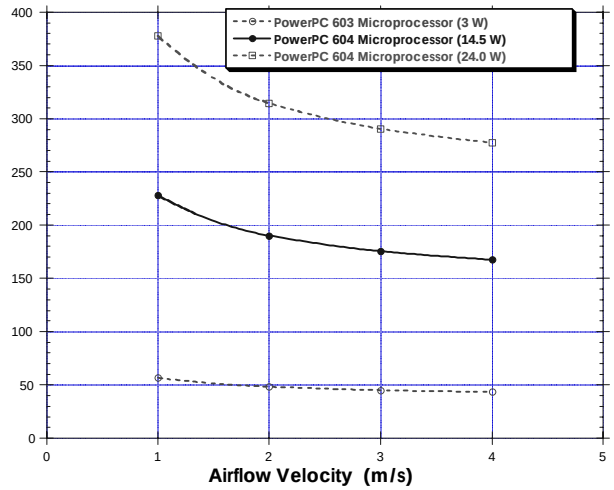

Figure 7. Model Results for the PowerPC 603 and PowerPC 604 Microprocessor (at 3 and 14.5, 24 watts; respectively) Temperature Rise above the Local Ambient with No Heat Sink.

was subdivided into cuboidal volumes. A progression in grid refinement was conducted, until grid independent temperatures were achieved.

Internal Package Conduction Resistance

For this C4/CBGA packaging technology, the intrinsic conduction thermal resistance paths are: 1) the die junction-to-case, and 2) the die junction-to-lead thermal resistance. These parameters are shown in Table 1; however, the use and limitations have been previously noted. In this C4/CBGA package, the silicon chip is exposed; therefore, the package "case" is the top of the silicon (Figure 2).

Table 1. C4/CBGA Internal-Package Thermal Conduction Resistance (3D model results)

Thermal Resistance	PowerPC 603 Microprocessor	PowerPC 604 Microprocessor
Die Junction-to-Case (eqn .4)	0.075 °C/W	0.0329 °C/W
Die Junction-to-Lead (eqn. 6)	3.4 °C/W	2.2 °C/W

Thermal Enhancement Options: Forced-air Cooling and Heat Sink Options

To validate the CFD models, experimental measurements were performed on the thermal test vehicle and were found to agree within approximately a 10% difference, over the range from natural convection to 4 m/s (Figure 6). Once the models of the test vehicle were validated, other models were generated for the PowerPC 603 and PowerPC 604 microprocessors. The worst-case power dissipations for the PowerPC 603 is 3 watts, while the PowerPC 604 microprocessors ranges from a typical of 14.5 at

100 MHz (processor core frequency) to 24.0 maximum at 133 MHz watts [1,2]. Next models were run for moderate air velocity, with the package mounted to a one-signal layer printed-

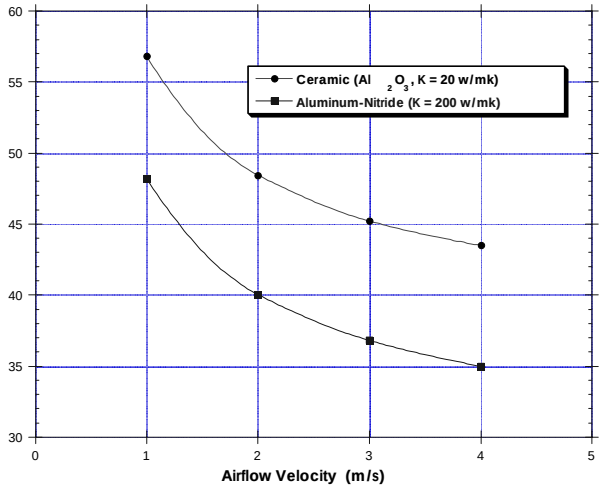

Figure 8. Model Results for the PowerPC 603 Microprocessor (3 watts) Temperature Rise above the Local Ambient with No Heat Sink for Alumina and Aluminum-Nitride Package Substrate Option.

circuit board with no heat sink which concurs with SEMI standards [12].

For the case when no heat sink is present for an air velocity of 1 m/s, the die-junction temperature rise above ambient was 60 °C for the PowerPC 603 microprocessor and is 230 °C for the PowerPC 604 microprocessor when operating at 14.5 watts.(Figure 7). Typical die-junction temperatures should be maintained less than 105 °C. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the computer cabinet before it reaches the component. A computer cabinet inlet-air temperature may range from 30 to 40°C. The air temperature rise within a cabinet may be in the range of 5 to 10°C. Thus, the allowable die-junction component temperature rise above ambient can range from 55 to 70 °C.

Clearly, the temperature rise for the PowerPC 604 microprocessor is too high and thermal enhancements need further investigation. First, the internal-package thermal conduction paths were examined. The junction-to-case is silicon and its contribution to the overall heat transfer path is less than 1%. Next, for the junction-to-lead thermal resistance, the effect of increasing the substrate conductivity an order-of-magnitude was considered (e.g., replacing the alumina ceramic (Al_2O_3 at 20 watt/meterK) with an aluminum-nitride ceramic (AlN at 200 watt/meterK). Using the PowerPC 603 microprocessor at 3 watts, its die-junction temperature rise is shown in Figure 8. This higher conductivity package substrate results in approximately a 15 to 20% reduction in the die-junction temperature rise. Thus, for moderate air-cooled computer systems, increasing package substrate conductivity has limited effect on reducing the die-junction temperature and this option alone would not be an effective thermal control option of the higher power dissipation of the PowerPC 604 microprocessor.

For the PowerPC 604 microprocessor, the addition of extended-surface heat sinking was the next consideration. A variety of commercially-available heat sinks were investigated for their

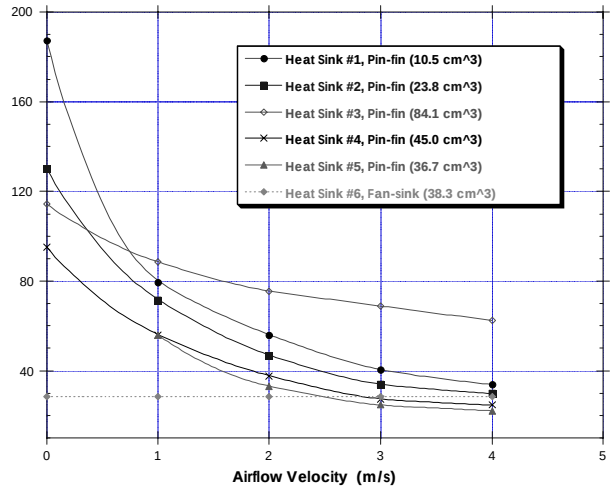

Figure 9. Model Results for the PowerPC 604 Microprocessor (14 watts) Die-junction temperature Rise for Various Heat Sink Options: Adiabatic Board .

thermal performance ([14] and Table 1, Appendix). For an adiabatic-board case, the temperature rise for the 14 watt PowerPC 604 microprocessor is shown in Figure 9. This graph may be used as an initial selection guide for a variety of boundary conditions; however, further modeling should be conducted at the system level and experimentally validated. Let us assume, for most computer systems in an office environment, a 60 °C die-junction component temperature rise above ambient is typical. Thus, three of the heat sinks would meet this criteria at 1 m/s of air velocity. If air velocity is increased further to 2 m/s, then five of the heat sinks meet this criteria. Of the passive heat sinks designs, the bi-directional offers the best thermal performance, for its relatively small spatial volume (Table 1, Appendix). The integral-fan pin-fin heat sink which promotes impingement airflow offers the best thermal performance; however, being an active device it requires external power. In addition, a system's designer might need to consider a "fail safe" thermal-control system in the event of a fan failure. Ultimately, the final selection of a heat sink and the thermal interface material depends on many factors, such as: thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

Board-level Component Population Considerations

Thermal performance data presented thus far, has been for a single component mounted to a one-signal layer card. Next, the board-level interaction effects of similarly powered neighboring components were considered. That is, board-level thermal flux would rise with increasing component population, thereby limiting the ability of the PCB to act as a heat sink.

Using the PowerPC 603 microprocessor at 3 watt power dissipation and an air velocity of 2 m/s (no heat sink), there was a considerable range in the die-junction component temperature rise, depending upon the board population (Figure 10). Figure 10 shows the die-junction temperature rise of the center component

on the PCB whether powered or not. The single C4/CBGA package had a die-junction temperature rise of approximately 50 °C, while for a board populated with all nine components (all powered at 3 watts), the center component temperature rise is

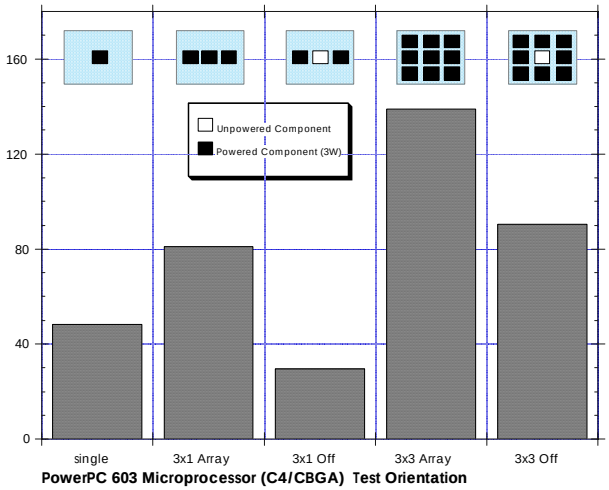

Figure 10. Model Results for the Populated Board Cases, Interaction Effects of the PowerPC 603 Microprocessor (3 watts) Temperature Rise above the Local Ambient with No Heat Sink.

approximately 135 °C. Notice, that even if the center component is not powered, the die-junction component temperature rise is 90°C. This example demonstrates the need for microelectronic thermal engineers to conduct board-level and system-level thermal simulations to accurately predict component operating temperature. In addition, due to the complex nature of heat transfer mechanisms, any models should be empirically validated.

SUMMARY AND CONCLUSIONS

As the intrinsic package thermal resistance for this C4/CBGA interconnect technology is quite low, proper thermal control design is primarily dependent upon the system-level design. This study has demonstrated the utility of using validated CFD models for parametric studies of various thermal management options for today's microelectronic systems. It has been shown that the three key parameters that affect, the die-junction temperature rise are: the board-level component population (i.e., thermal loading), the heat sink style and design, and the air velocity. First, as the board-level component population increases, the ability for the PCB to act like a "heat sink" is diminished. Next, the heat sink size and its design affect the amount of heat that might be removed from the C4/CBGA package. Finally the air velocity on the components and/or the heat sink determine the die junction temperature rise.

The following conclusions are noted:

1) For airflow velocities from 1 to 2 m/s, the PowerPC 603 microprocessor, may not require heat sinking; however, heatsinking may be required if the PCB board has high thermal loading.

2) For the PowerPC 603 microprocessor, use of a high thermal conductivity aluminum-nitride substrate, reduces the die-junction temperature rise by approximately 15 to 20%. However, the higher conductivity substrate would be less effective as board-level thermal flux increases.

3) The PowerPC 604 microprocessor will require heat sinking to maintain its die-junction temperature less than 105 °C. Of the passive heat sinks designs the bi-directional offered the best thermal performance for its spatial volume. Note, due to silicon die fragility any heat sink attach material must be structurally compliant.

The component supplier may suggest a die-junction temperature for adequate reliability and electrical performance. But of all the parameters determining the die-junction temperature, a component supplier can only control the chip power and the internal package resistance. The system-level thermal resistances are often the governing terms of the junction-to-ambient thermal resistance. Thus, the system-level thermal design plays a significant role in achieving the component supplier's recommended die-junction operating temperature.

These results are considered to be within +/- 10%. As noted here, due to the complexity of the heat transfer paths, any modeling should be confirmed with experimental results for the system-level boundary conditions.

ACKNOWLEDGMENTS

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APPENDIX

Table 1. Active and Passive Heat Sinks

Heat Sink Number	Heat Sink Style	*Depth (mm)*	*Width (mm)*	*Height (mm)*	*Volume (mm^3)*
1	Pin-fin	24.76	27.94	15.24	10,542.95
2	Pin-fin	37.97	38.10	16.51	23,884.31
3	Stamped	58.00	58.00	25.00	84,100.00
4	Pin-fin	51.20	53.30	16.50	45,027.84
5	Bi-directional	38.00	38.00	25.40	36,677.60
6	Fan sink (12 volt)	38.00	38.00	26.50	38,266.00

Table 2.0 PowerPC 603 and PowerPC 604 RISC Microprocessors [1,2]

Microprocessor	*Transistors*	*Performance SPECint92/ SPECfp92*	*Power Typical/Maximum Dissipation (watt)*	*Die Size (mm)*	*CBGA Substrate Size (mm)*	*CBGA Substrate Leads*
PowerPC 603	1.6 million	160/140	1 to 3 @80 MHz	7.5x11.5	21x21	255
PowerPC 604	3.6 million	225/250	14.5 to 24 @100 - 133MHz	12.4x15.8	21x21	255

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