1. General description

UCODE 7m is a derivative of the UCODE 7 and offers on top of the UCODE 7 features a 32-bit User Memory.

NXP’s UCODE 7m IC is the leading-edge EPC Gen2 RFID chip that offers best-in-class performance and features for use in the most demanding RFID tagging applications.

Particularly well suited for inventory management application, like e.g. Retail and Fashion, with its leading edge RF performance for any given form factor, UCODE 7m enables long read distance and fast inventory of dense RFID tag population. With its broadband design, it offers the possibility to manufacture true global RFID label with best-in-class performance over worldwide regulations.

The device also provides an automatic self pre-serialization feature for 96-bit EPC, following the industry aligned Multi Vendor Chip-based serialization scheme, and a Parallel encoding feature. For applications where the same 58-bit Stock Keeping Unit (SKU) needs to be encoded on multiple tags, at the same time, a combination of both features improves and simplifies the tag initialization process.

On top UCODE 7m offers a Tag Power Indicator for RFID tag initialization optimization and a Product Status Flag for Electronic Article Surveillance (EAS) application.

2. Features and benefits

2.1 Key features

- Read sensitivity -21 dBm
- Write sensitivity -16 dBm
- Parallel encoding mode: 100 items in 60ms
- Encoding speed: 16 bits per millisecond
- Innovative functionalities
  - Tag Power Indicator
  - Automatic self pre-serialization for 96-bit EPC
  - Integrated Product Status Flag (PSF)
- Compatible with single-slit antenna
- Up to 128-bit EPC
- 96-bit Unique Tag Identifier (TID) factory locked, including 48-bit unique serial number
- 32-bit User Memory
- EPC Gen2 v2.0 ready
2.1.1 Memory
- 32-bit User Memory
- Up to 128-bit of EPC memory
- Supports self pre-serialization for 96-bit EPC
- 96-bit Tag IDentifier (TID) factory locked
- 48-bit unique serial number factory-encoded into TID
- 32-bit access password
- Wide operating temperature range: \(-40^\circ C\) up to \(+85^\circ C\)
- Minimum 100,000 write cycle endurance

2.2 Key benefits

2.2.1 End user benefit
- Long READ and WRITE ranges due to leading edge chip sensitivity
- Very fast bulk encoding
- Product identification through unalterable extended TID range, including a 48-bit serial number
- Reliable operation in dense reader and noisy environments through high interference rejection

2.2.2 Antenna design benefits
- High sensitivity enables smaller and cost efficient antenna designs for the same retail category
- Tag Power Indicator features enables very high density of inlay on rolls without cross-talk issues during writing/encoding
- The different input capacitance for the single slit antenna solution enables a finer tuning of the impedance for the antenna design

2.2.3 Label manufacturer benefit
- Large RF pad-to-pad distance to ease antenna design
- Symmetric RF inputs are less sensitive to process variation
- Single slit antenna for a more mechanically stable antenna connection
- Automatic self pre-serialization of the 96-bit EPC anytime its EPC serial number is erased
- Extremely fast encoding of the EPC content

2.3 Supported features
- All mandatory commands of EPC global specification V.1.2.0 are implemented including:
  - (Perma)LOCK
- The following optional commands are implemented in conformance with the EPC specification:
  - Access
  - BlockWrite (2 words, 32-bit)
Product Status Flag bit: enables the UHF RFID tag to be used as EAS (Electronic Article Surveillance) tag without the need for a back-end data base.

Tag Power Indicator: enables the reader to select only ICs/tags that have enough power to be written to.

Parallel encoding: allows for the ability to bring (multiple) tag(s) quickly to the OPEN state and hence allowing single tags to be identified simply, without timing restrictions, or multiple tags to be e.g. written to at the same time, considerably reducing the encoding process.

All supported features of UCODE 7m can be activated using standard EPCglobal READ / WRITE / ACCESS / SELECT commands. No custom commands are needed to take advantage of all the features in case of unlocked EPC memory. The parallel encoding feature may however require a firmware upgrade of the reader to use its full potential.

3. Applications

3.1 Markets

- Retail/Fashion (apparel, footwear, jewelry, cosmetics)
- Fast Moving Consumer Goods

3.2 Applications

- Retail Inventory management
- Supply chain management
- Loss prevention
- Asset management

Outside the applications mentioned above, please contact NXP Semiconductors for support.

4. Ordering information

Table 1. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package Name</th>
<th>IC type</th>
<th>Description</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>SL3S1214FUD/BG</td>
<td>Wafer</td>
<td>UCODE 7m</td>
<td>bumped die on sawn 8&quot; 120 μm wafer 7 μm Polyimide spacer</td>
<td>not applicable</td>
</tr>
</tbody>
</table>
5. Block diagram

The SL3S1214 IC consists of three major blocks:

- Analog Interface
- Digital Control
- EEPROM

The analog part provides stable supply voltage and demodulates data received from the reader which is then processed by the digital part. Further, the modulation transistor of the analog part transmits data back to the reader.

The digital section includes the state machines, processes the protocol and handles communication with the EEPROM, which contains the EPC and the user data.

![Block diagram of UCODE 7m IC](image-url)
6. Pinning information

![Pinning bare die](image)

Fig 2. Pinning bare die

6.1 Pin description

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TP1</td>
<td>test pad 1</td>
</tr>
<tr>
<td>RF1</td>
<td>antenna connector 1</td>
</tr>
<tr>
<td>TP2</td>
<td>test pad 2</td>
</tr>
<tr>
<td>RF2</td>
<td>antenna connector 2</td>
</tr>
</tbody>
</table>
7. Wafer layout

7.1 Wafer layout

(1) Die to Die distance (metal sealring - metal sealring) 21.4 µm, (X-scribe line width: 15 µm)
(2) Die to Die distance (metal sealring - metal sealring) 21.4 µm, (Y-scribe line width: 15 µm)
(3) Chip step, x-length: 460 µm
(4) Chip step, y-length: 505 µm
(5) Bump to bump distance X (TP1 - RF2): 358 µm
(6) Bump to bump distance Y (RF1 - RF2): 403 µm
(7) Distance bump to metal sealring X: 40.3 µm (outer edge - top metal)
(8) Distance bump to metal sealring Y: 40.3 µm

Bump size X x Y: 60 µm x 60 µm

Remark: TP1 and TP2 are physically disconnected

Fig 3. UCODE 7m wafer layout
8. Mechanical specification

The UCODE 7m wafer is available in 120 μm thickness with 7 μm Polyimide spacer.

8.1 Wafer specification

See Ref. 21 "Data sheet - Delivery type description – General specification for 8" wafer on UV-tape with electronic fail die marking, BU-ID document number: 1093**".

8.1.1 Wafer

Table 3. Specifications

<table>
<thead>
<tr>
<th>Wafer</th>
<th>Designation</th>
<th>each wafer is scribed with batch number and wafer number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diameter</td>
<td>200 mm (8&quot;) unsawn - 205 mm typical sawn on foil</td>
<td></td>
</tr>
<tr>
<td>Thickness</td>
<td>SL3S1214FUD/BG</td>
<td>120 μm ± 15 μm</td>
</tr>
<tr>
<td>Number of pads</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>Pad location</td>
<td>non diagonal / placed in chip corners</td>
<td></td>
</tr>
<tr>
<td>Distance pad to pad RF1-RF2</td>
<td>403.0 μm</td>
<td></td>
</tr>
<tr>
<td>Distance pad to pad TP1-RF2</td>
<td>358.0 μm</td>
<td></td>
</tr>
<tr>
<td>Process</td>
<td>CMOS 0.14 μm</td>
<td></td>
</tr>
<tr>
<td>Batch size</td>
<td>25 wafers</td>
<td></td>
</tr>
<tr>
<td>Potential good dies per wafer</td>
<td>126.524</td>
<td></td>
</tr>
</tbody>
</table>

Wafer backside

| Material | Si |
| Treatment | ground and stress release |
| Roughness | Rₐ max. 0.5 μm, Rₙ max. 5 μm |

Chip dimensions

| Die size excluding scribe | 0.490 mm × 0.445 mm = 0.218 mm² |
| Scribe line width | x-dimension = 15 μm |
| | y-dimension = 15 μm |

Passivation on front

| Type | Sandwich structure |
| Material | PE-Nitride (on top) |
| Thickness | 1.75 μm total thickness of passivation |
| Polyimide spacer | 7 μm ± 1 μm (SL3S1214FUD/BG only) |

Au bump

| Bump material | > 99.9 % pure Au |
| Bump hardness | 35 – 80 HV 0.005 |
| Bump shear strength | > 70 MPa |
| Bump height | 25 μm [1] |
8.1.2 Fail die identification

No ink dots are applied to the wafer.

Electronic wafer mapping (SECS II format) covers the electrical test results and additionally the results of mechanical/visual inspection.

See Ref. 21 "Data sheet - Delivery type description – General specification for 8" wafer on UV-tape with electronic fail die marking, BU-ID document number: 1093***"

8.1.3 Map file distribution

See Ref. 21 "Data sheet - Delivery type description – General specification for 8" wafer on UV-tape with electronic fail die marking, BU-ID document number: 1093***"

9. Functional description

9.1 Air interface standards

The UCODE 7m fully supports all parts of the "Specification for RFID Air Interface EPCglobal, EPC Radio-Frequency Identity Protocols, Class-1 Generation-2 UHF RFID, Protocol for Communications at 860 MHz to 960 MHz, Version 1.2.0".

9.2 Power transfer

The interrogator provides an RF field that powers the tag, equipped with a UCODE 7m. The antenna transforms the impedance of free space to the chip input impedance in order to get the maximum possible power for the UCODE 7m on the tag.

The RF field, which is oscillating on the operating frequency provided by the interrogator, is rectified to provide a smoothed DC voltage to the analog and digital modules of the IC.

The antenna that is attached to the chip may use a DC connection between the two antenna pads. Therefore the UCODE 7m also enables loop antenna design.
9.3 Data transfer

9.3.1 Interrogator to tag Link
An interrogator transmits information to the UCODE 7m by modulating an UHF RF signal. The UCODE 7m receives both information and operating energy from this RF signal. Tags are passive, meaning that they receive all of their operating energy from the interrogator’s RF waveform.

An interrogator is using a fixed modulation and data rate for the duration of at least one inventory round. It communicates to the UCODE 7m by modulating an RF carrier.

For further details refer to Ref. 1. Interrogator-to-tag (R=>T) communications.

9.3.2 Tag to interrogator Link
Upon transmitting a valid command an interrogator receives information from a UCODE 7m tag by transmitting an unmodulated RF carrier and listening for a backscattered reply. The UCODE 7m backscatters by switching the reflection coefficient of its antenna between two states in accordance with the data being sent. For further details refer to Ref. 1, chapter 6.3.1.3.

The UCODE 7m communicates information by backscatter-modulating the amplitude and/or phase of the RF carrier. Interrogators shall be capable of demodulating either demodulation type.

The encoding format, selected in response to interrogator commands, is either FM0 baseband or Miller-modulated subcarrier.

9.4 Supported commands
The UCODE 7m supports all mandatory EPCglobal V1.2.0 commands including

- (perma) LOCK command

In addition the UCODE 7m supports the following optional commands:

- ACCESS
- Block Write (32 bit)

The Kill Password of the UCODE 7m is zero-valued and permanent read/write locked, which disallows the IC from being killed.
9.5 UCODE 7m memory

The UCODE 7m memory is implemented according EPCglobal Class1Gen2 and organized in three sections:

Table 4. UCODE 7m memory sections

<table>
<thead>
<tr>
<th>Name</th>
<th>Size</th>
<th>Bank</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved memory (32-bit Kill password and 32-bit Access password)</td>
<td>64 bit</td>
<td>00b</td>
</tr>
<tr>
<td>EPC (excluding 16 bit CRC-16 and 16 bit PC)</td>
<td>128 bit</td>
<td>01b</td>
</tr>
<tr>
<td>UCODE 7m Configuration Word</td>
<td>16 bit</td>
<td>01b</td>
</tr>
<tr>
<td>TID (including permalocked unique 48 bit serial number)</td>
<td>96 bit</td>
<td>10b</td>
</tr>
<tr>
<td>User Memory</td>
<td>32 bit</td>
<td>11b</td>
</tr>
</tbody>
</table>

The logical address of all memory banks begin at zero (00h).

In addition to the four memory banks one configuration word to handle the UCODE 7m specific features is available at EPC bank 01 address bit-200h. The configuration word is described in detail in 9.6.

The TID complies to the extended tag Identification scheme according GS1 EPC Tag Data Standard 1.6.

The EPC content will follow a self pre-serialization scheme following the Multi Vendor Chip-based serialization scheme (Ref. 23) see Section 9.6.3 “Automatic self pre-serialization of the 96-bit EPC” for more details.
### 9.5.1 UCODE 7m overall memory map

<table>
<thead>
<tr>
<th>Bank address</th>
<th>Memory address</th>
<th>Type</th>
<th>Content</th>
<th>Initial</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bank 00</td>
<td>00h to 1Fh</td>
<td>reserved</td>
<td>Kill password</td>
<td>hard wired 00h</td>
<td>permanent read/write locked</td>
</tr>
<tr>
<td></td>
<td>20h to 3Fh</td>
<td>reserved</td>
<td>Access password</td>
<td>all 00h</td>
<td>unlocked memory</td>
</tr>
<tr>
<td>Bank 01 EPC</td>
<td>00h to 0Fh</td>
<td>EPC</td>
<td>CRC-16: refer to Ref. 17</td>
<td>memory mapped calculated CRC</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10h to 14h</td>
<td>EPC</td>
<td>EPC length</td>
<td>00110b</td>
<td>unlocked memory</td>
</tr>
<tr>
<td></td>
<td>15h</td>
<td>EPC</td>
<td>UMI</td>
<td>0b</td>
<td>unlocked memory</td>
</tr>
<tr>
<td></td>
<td>16h</td>
<td>EPC</td>
<td>XPC indicator</td>
<td>0b</td>
<td>hardwired to 0</td>
</tr>
<tr>
<td></td>
<td>17h to 1Fh</td>
<td>EPC</td>
<td>numbering system indicator</td>
<td>00h</td>
<td>unlocked memory</td>
</tr>
<tr>
<td>Bank 01 Config Word</td>
<td>200h</td>
<td>EPC</td>
<td>RFU</td>
<td>0b</td>
<td>locked memory</td>
</tr>
<tr>
<td></td>
<td>201h</td>
<td>EPC</td>
<td>RFU</td>
<td>0b</td>
<td>locked memory</td>
</tr>
<tr>
<td></td>
<td>202h</td>
<td>EPC</td>
<td>Parallel encoding</td>
<td>0b</td>
<td>Action bit[4]</td>
</tr>
<tr>
<td></td>
<td>203h</td>
<td>EPC</td>
<td>RFU</td>
<td>0b</td>
<td>locked memory</td>
</tr>
<tr>
<td></td>
<td>204h</td>
<td>EPC</td>
<td>Tag Power Indicator</td>
<td>0b</td>
<td>Action bit[4]</td>
</tr>
<tr>
<td></td>
<td>205h</td>
<td>EPC</td>
<td>RFU</td>
<td>0b</td>
<td>locked memory</td>
</tr>
<tr>
<td></td>
<td>206h</td>
<td>EPC</td>
<td>RFU</td>
<td>0b</td>
<td>locked memory</td>
</tr>
<tr>
<td></td>
<td>207h</td>
<td>EPC</td>
<td>RFU</td>
<td>0b</td>
<td>locked memory</td>
</tr>
<tr>
<td></td>
<td>208h</td>
<td>EPC</td>
<td>RFU</td>
<td>0b</td>
<td>locked memory</td>
</tr>
<tr>
<td></td>
<td>209h</td>
<td>EPC</td>
<td>max. backscatter strength</td>
<td>1b</td>
<td>permanent bit[5]</td>
</tr>
<tr>
<td></td>
<td>20Ah</td>
<td>EPC</td>
<td>RFU</td>
<td>0b</td>
<td>locked memory</td>
</tr>
<tr>
<td></td>
<td>20Bh</td>
<td>EPC</td>
<td>RFU</td>
<td>0b</td>
<td>locked memory</td>
</tr>
<tr>
<td></td>
<td>20Ch</td>
<td>EPC</td>
<td>RFU</td>
<td>0b</td>
<td>locked memory</td>
</tr>
<tr>
<td></td>
<td>20Dh</td>
<td>EPC</td>
<td>RFU</td>
<td>0b</td>
<td>locked memory</td>
</tr>
<tr>
<td></td>
<td>20Fh</td>
<td>EPC</td>
<td>PSF alarm flag</td>
<td>0b</td>
<td>Permanent bit[5]</td>
</tr>
<tr>
<td>Bank 10 TID</td>
<td>00h to 07h</td>
<td>TID</td>
<td>allocation class identifier</td>
<td>1110 0010b</td>
<td>locked memory</td>
</tr>
<tr>
<td></td>
<td>08h to 13h</td>
<td>TID</td>
<td>tag mask designer identifier</td>
<td>1000 0000 0110b</td>
<td>locked memory</td>
</tr>
<tr>
<td></td>
<td>14h</td>
<td>TID</td>
<td>config word indicator</td>
<td>1b[2]</td>
<td>locked memory</td>
</tr>
<tr>
<td></td>
<td>14h to 1Fh</td>
<td>TID</td>
<td>tag model number</td>
<td>TMNR[3]</td>
<td>locked memory</td>
</tr>
<tr>
<td></td>
<td>20h to 2Fh</td>
<td>TID</td>
<td>XTID header</td>
<td>2000h</td>
<td>locked memory</td>
</tr>
<tr>
<td></td>
<td>30h to 5Fh</td>
<td>TID</td>
<td>Serial Number</td>
<td>SNR</td>
<td>locked memory</td>
</tr>
<tr>
<td>Bank 11 User Memory</td>
<td>00h to 1Fh</td>
<td>UM</td>
<td>User memory</td>
<td>all 00h</td>
<td>unlocked memory</td>
</tr>
</tbody>
</table>

[1] HEX E280 6811 0000 00nn nnnn nnn (0000 0000) where n are the bytes used for the pre-serialized EPC. see also Section 9.6.3
[2] Indicates the existence of a Configuration Word at the end of the EPC number
[3] See Figure 4
[4] Action bits: meant to trigger a feature upon a SELECT command on the related bit, see Section 9.6.1
[5] Permanent bit: permanently stored bits in the memory; Read/Writeable according EPC bank lock status, see Section 9.6.1
9.5.2  UCODE 7m TID memory details

<table>
<thead>
<tr>
<th>First 48 bit of TID memory</th>
<th>Class ID</th>
<th>Mask Designer ID</th>
<th>Model Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>UCODE 7m</td>
<td>028068112000</td>
<td>E2h</td>
<td>0010001000000000h</td>
</tr>
</tbody>
</table>

Fig 4. UCODE 7m TID memory structure


9.6 Supported features

The UCODE 7m is equipped with a number of additional features, which are implemented in such a way that standard EPCglobal READ / WRITE / ACCESS / SELECT commands can be used to operate these features.

The Configuration Word, as mentioned in the memory map, describes the additional features located at address 200h of the EPC memory.

Bit 14h of the TID indicates the existence of a Configuration Word. This flag will enable the selection of configuration word enhanced transponders in mixed tag populations.

Please refer to Ref. 22 for additional reference.

9.6.1 UCODE 7m features control mechanism

The different features of the UCODE 7m can be activated / de-activated by addressing or changing the content of the corresponding bit in the configuration word located at address 200h in the EPC memory bank (see Table 6). The de-activation of the action bit features will only happen after chip reset.

Table 6. Configuration word UCODE 7m

<table>
<thead>
<tr>
<th>Locked memory</th>
<th>Action bit</th>
<th>Locked memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>RFU</td>
<td>RFU</td>
<td>Parallel encoding</td>
</tr>
<tr>
<td>0 1 2 3 4 5 6 7</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 7. Configuration word UCODE 7m ... continued

<table>
<thead>
<tr>
<th>Locked memory</th>
<th>Permanent bit</th>
<th>Locked memory</th>
<th>Permanent bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>RFU</td>
<td>max. backscatter strength</td>
<td>RFU</td>
<td>RFU</td>
</tr>
<tr>
<td>8 9 10 11 12 13 14 15</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The configuration word contains 2 different type of bits:

- **Action bits**: meant to trigger a feature upon a SELECT command on the related bit:
  - Parallel encoding
  - Tag Power indicator

- **Permanent bits**: permanently stored bits in the memory
  - Max. Backscatter Strength
  - PSF Alarm bit

The activation or the de-activation of the feature behind the permanent bits happens only when attempting to write a “1” value to the related bit (value toggling) - writing “0” value will have no effect.

If the feature is activated, the related bit will be read with a “1” value and, if de-activated, with a “0” value.

The permanent bits can only be toggled using standard EPC WRITE if the EPC bank is unlocked or within the SECURED state if the EPC is locked. If the EPC is perma locked, they cannot be changed.
Action bits will trigger a certain action only if the pointer of the SELECT command exactly matches the action-bit address (i.e. 202h or 204h), if the length=1 and if mask=1b (no multiple trigger of actions possible within one single SELECT command).

After issuing a SELECT to any action bits an interrogator shall transmit CW for RTCal $Ref. \, 9 + 80 \mu s$ before sending the next command.

If the truncate bit in the SELECT command is set to "1" the SELECT will be ignored.

A SELECT on action bits will not change the digital state of the chip.

The action bits can be triggered regardless if the EPC memory is unlocked, locked or perma locked.

9.6.2 Backscatter strength reduction

The UCODE 7m features two levels of backscatter strengths. Per default maximum backscatter is enabled in order to enable maximum read rates. When clearing the flag the strength can be reduced if needed.

9.6.3 Automatic self pre-serialization of the 96-bit EPC

![Automatic self pre-serialization scheme for 96-bit EPC](image)
Fig 6. Illustration of the handling of the EPC self-preserialization
Description

In case the EPC length is set to be 96-bit, the EPC is by default self pre-serialized following a 96-bit EPC serialization scheme according to the Multi Vendor Chip-based serialization guideline (see Ref. 23), meaning the lower 38-bit will always contain 3 bits for the manufacturer code (111 for NXP) and 35 bit serial number taken from the lower 35 bits of the TID serial number (see Figure 5).

As long as the initial content of the lower 38-bit of the EPC is not changed, the EPC will appear serialized. As soon as any of those 38 bits are written, the EPC will show the written content.

Once the pre-serialization of the EPC is overwritten and the EPC is not locked, the self pre-serialization can be re-activated by one of the following ways:

- Setting the 38-bit Serial number of the EPC to “0” (see Figure 5), or
- Erase sixth and fifth word of the EPC to “00 00h” and keep the content of the lower 6 bits of the fourth word of the EPC at its serialized content (see Figure 6).

The self pre-serialization only applies to an EPC length of 96 bits, which is the initial EPC length settings of UCODE 7m.

Use cases and benefits

This automatic EPC serialization is meant to be able to guarantee a unique EPC number for each tagged items even if the same Stock Keeping Unit (SKU) is used. By being serialized by default, the encoding process of the tags with UCODE 7m gets simpler and faster as it only needs to encode the SKU (58-bit header of the EPC).

9.6.4 Parallel encoding

Description

This feature of the UCODE 7m can be activated by the “Parallel encoding bit” in the Configuration-Word located at (202h).

Upon issuing a EPC SELECT command on the “Parallel encoding bit”, in a population of UCODE 7m tags, a subsequent QUERY brings all tags go the OPEN state with a specific handle (“AAAAh”).

Once in the OPEN state, for example a WRITE command will apply to all tags in the OPEN state (see Figure 8). This parallel encoding is considerably lowering the encoding time compared to a standard implementation (see Figure 7).

The amount of tags that can be encoded at the same time will depend on the strength of the reader signal. Since all tags will backscatter their ACKNOWLEDGE (ACK) response at the same time, the reader will observe collision in the signal from the tags.
Fig 7. Example of 16-bit Write command with standard EPC Gen 2 commands

- Only TAG 1 is being addressed
- Only TAG 2 is being addressed
### Use cases and benefits

Parallel encoding feature of UCODE 7m can enable ultra fast bulk encoding.

Taking in addition advantage of the pre-serialization scheme of UCODE 7m, the same SKU can be encoded in multiple tags as the EPC will be delivered pre-serialized already.

In the case of only one tag answering (like in printer encoding), this feature could be used to save some overhead in commands to do direct EPC encoding after the handle reply.

Since this is a UCODE 7m specific feature the use of this features requires support on the reader side.

### 9.6.5 Tag Power Indicator

#### Description

Upon a SELECT command on the “Tag Power Indicator”, located in the config word 204h, an internal power check on the chip is performed to see if the power level is sufficient to perform a WRITE command. The decision level is defined as nominal WRITE sensitivity minus 1dB. In the case there is enough power, the SELECT command is matching and non-matching if not enough power. The tag can then be singulated by the standard inventory procedure.
Use cases and benefits

This feature gives the possibility to select only the tag(s) that receive enough power to be written during e.g. printer encoding in a dense environment of tags even though the reader may read more than one tag (see Figure 9 for illustration). The power level still needs to be adjusted to transmit enough writing power to one tag only to do one tag singulation.

Fig 9. Selection of tags with Tag Power Indicator feature
9.6.6 **Product Status Flag (PSF)**

**Description**

The PSF is a general purpose bit located in the Configuration word at address 20Fh with a value that can be freely changed.

**Use cases and benefits**

The PSF bit can be used as an EAS (Electronic Article Surveillance) flag, quality checked flag or similar.

In order to detect the tag with the PSF activated, a EPC SELECT command selecting the PSF flag of the Configuration word can be used. In the following inventory round only PSF enabled chips will reply their EPC number.

9.6.7 **Single-slit antenna solution**

**Description**

In UCODE 7m the test pads TP1 and TP2 are electrically disconnected meaning they are not electrically active and can be safely short-circuited to the RF pads RF1 and RF2 (see Figure 10).

**Uses cases and benefits**

Using single-slit antenna enables easier assembly and antenna design. Inlay manufacturer will only have to take care about one slit of the antenna instead of two in case all pads need to be disconnected from each other.

Additionally single-slit antenna assembly and the related increased input capacitance (see Table 9) can be used advantageously over the standard antenna design as additional room for optimization to different antenna design.
## 10. Limiting values

Table 8. Limiting values[1][2][3]

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to RFN

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>Bare die limitations</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>storage temperature</td>
<td>-55</td>
<td>+125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>$T_{amb}$</td>
<td>ambient temperature</td>
<td>-40</td>
<td>+85</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>$V_{ESD}$</td>
<td>electrostatic discharge voltage</td>
<td>Human body model</td>
<td>-</td>
<td>± 2</td>
<td>kV</td>
</tr>
<tr>
<td></td>
<td><strong>Pad limitations</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$P_i$</td>
<td>input power</td>
<td>maximum power</td>
<td>-</td>
<td>100</td>
<td>mW</td>
</tr>
</tbody>
</table>

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Operating Conditions and Electrical Characteristics section of this specification is not implied.

[2] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.

[3] For ESD measurement, the die chip has been mounted into a CDIP20 package.
11. Characteristics

11.1 UCODE 7m bare die characteristics

Table 9. UCODE 7m RF interface characteristics (RF1, RF2)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>fi</td>
<td>input frequency</td>
<td>840 - 960 MHz</td>
<td>840</td>
<td>-</td>
<td>960</td>
<td>MHz</td>
</tr>
<tr>
<td>Pi(min)</td>
<td>minimum input power</td>
<td>READ sensitivity</td>
<td>-21</td>
<td>-</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td>Pi(min)</td>
<td>minimum input power</td>
<td>WRITE sensitivity</td>
<td>-16</td>
<td>-</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td>t 16bit</td>
<td>encoding speed</td>
<td>16-bit</td>
<td>-1</td>
<td>1</td>
<td>-</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>32-bit (block write)</td>
<td>-1</td>
<td>1.8</td>
<td>-</td>
<td>ms</td>
</tr>
<tr>
<td>Ci</td>
<td>chip input capacitance</td>
<td>parallel</td>
<td>0.63</td>
<td>-</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>Z</td>
<td>chip impedance</td>
<td>866 MHz</td>
<td>14.5-j293</td>
<td>-</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>915 MHz</td>
<td>12.5-j277</td>
<td>-</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>953 MHz</td>
<td>12.5-j267</td>
<td>-</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td></td>
<td>typical assembled impedance</td>
<td>915MHz</td>
<td>18-j245</td>
<td>-</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td></td>
<td>typical assembled impedance</td>
<td>in case of single-slit antenna assembly</td>
<td>915MHz</td>
<td>13.5-j195</td>
<td>-</td>
<td>Ω</td>
</tr>
</tbody>
</table>

Table 10. UCODE 7m memory characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>tret</td>
<td>retention time</td>
<td>T_{amb} ≤ 55 °C</td>
<td>20</td>
<td>-</td>
<td>-</td>
<td>year</td>
</tr>
<tr>
<td>N_{endu(W)}</td>
<td>write endurance</td>
<td>100k</td>
<td>-</td>
<td>-</td>
<td>cycle</td>
<td></td>
</tr>
</tbody>
</table>
12. Package outline

This section is not applicable for this kind of device.

13. Packing information

13.1 Wafer

See Ref. 21 "Data sheet - Delivery type description – General specification for 8” wafer on UV-tape with electronic fail die marking, BU-ID document number: 1093***

14. Abbreviations

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CRC</td>
<td>Cyclic Redundancy Check</td>
</tr>
<tr>
<td>CW</td>
<td>Continuous Wave</td>
</tr>
<tr>
<td>DSB-ASK</td>
<td>Double Side Band-Amplitude Shift Keying</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>EAS</td>
<td>Electronic Article Surveillance</td>
</tr>
<tr>
<td>EEPROM</td>
<td>Electrically Erasable Programmable Read Only Memory</td>
</tr>
<tr>
<td>EPC</td>
<td>Electronic Product Code (containing Header, Domain Manager, Object Class and Serial Number)</td>
</tr>
<tr>
<td>FM0</td>
<td>Bi phase space modulation</td>
</tr>
<tr>
<td>G2</td>
<td>Generation 2</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>PIE</td>
<td>Pulse Interval Encoding</td>
</tr>
<tr>
<td>PSF</td>
<td>Product Status Flag</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>UHF</td>
<td>Ultra High Frequency</td>
</tr>
<tr>
<td>SECS</td>
<td>Semi Equipment Communication Standard</td>
</tr>
<tr>
<td>TID</td>
<td>Tag IDentifier</td>
</tr>
</tbody>
</table>
15. References


[2] EPCglobal: EPC Tag Data Standards


[6] European Telecommunications Standards Institute (ETSI), EN 302 208: Electromagnetic compatibility and radio spectrum matters (ERM) – Radio-frequency identification equipment operating in the band 865 MHz to 868 MHz with power levels up to 2 W, Part 2 – Harmonised EN under article 3.2 of the R&TTE directive

[7] [CEPT1]: CEPT REC 70-03 Annex 1

[8] [ETSI1]: ETSI EN 330 220-1, 2

[9] RTCal is the Interrogator-to-Tag calibration symbol length defined in the EPCglobal specification


[11] [FCC1]: FCC 47 Part 15 Section 247


[21] Data sheet - Delivery type description – General specification for 8” wafer on UV-tape with electronic fail die marking, BU-ID document number: 1093**1

[22] Application note - AN11274 – FAQ on UCODE 7

[23] Release Note - Formulas for Multi-Vendor Chip-Based Serialization (MCS) and FastEPC, BU-ID document number: 2498**

1. ** ... document version number
# 16. Revision history

<table>
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<tr>
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<th>Release date</th>
<th>Data sheet status</th>
<th>Change notice</th>
<th>Supersedes</th>
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<tr>
<td>SL3S1214 v. 3.0</td>
<td>20141023</td>
<td>Product data sheet</td>
<td>-</td>
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17. Legal information

17.1 Data sheet status

<table>
<thead>
<tr>
<th>Document status</th>
<th>Product status</th>
<th>Definition</th>
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<tr>
<td>Objective [short] data sheet</td>
<td>Development</td>
<td>This document contains data from the objective specification for product development.</td>
</tr>
<tr>
<td>Preliminary [short] data sheet</td>
<td>Qualification</td>
<td>This document contains data from the preliminary specification.</td>
</tr>
<tr>
<td>Product [short] data sheet</td>
<td>Production</td>
<td>This document contains the product specification.</td>
</tr>
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</table>

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL: http://www.nxp.com.

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18. Contact information

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For sales office addresses, please send an email to: salesaddresses@nxp.com
19. Contents

1 General description ............................................. 1
2 Features and benefits ........................................... 1
  2.1 Key features ................................................ 1
  2.1.1 Memory .................................................. 2
  2.2 Key benefits ............................................... 2
  2.2.1 End user benefit ....................................... 2
  2.2.2 Antenna design benefits ................................ 2
  2.2.3 Label manufacturer benefit ........................... 2
  2.3 Supported features ....................................... 2
3 Applications .................................................. 3
  3.1 Markets ...................................................... 3
  3.2 Applications .............................................. 3
4 Ordering information ........................................... 3
5 Block diagram ................................................ 4
6 Pinning information ............................................ 5
  6.1 Pin description ............................................. 5
7 Wafer layout .................................................. 6
  7.1 Wafer layout ................................................. 6
8 Mechanical specification ....................................... 7
  8.1 Wafer specification ......................................... 7
  8.1.1 Wafer .................................................... 7
  8.1.2 Fail die identification .................................. 8
  8.1.3 Map file distribution ................................. 8
9 Functional description ........................................ 8
  9.1 Air interface standards .................................... 8
  9.2 Power transfer ............................................ 8
  9.3 Data transfer ................................................ 9
  9.3.1 Interrogator to tag Link ................................ 9
  9.3.2 Tag to interrogator Link ................................ 9
  9.4 Supported commands ...................................... 9
  9.5 UCODE 7m memory ......................................... 10
  9.5.1 UCODE 7m overall memory map ...................... 11
  9.5.2 UCODE 7m TID memory details ...................... 12
  9.6 Supported features ...................................... 13
  9.6.1 UCODE 7m features control mechanism ................ 13
  9.6.2 Backscatter strength reduction ...................... 14
  9.6.3 Automatic self pre-serialization of the 96-bit EPC ................................................ 14
    Description ................................................. 16
    Use cases and benefits .................................... 16
  9.6.4 Parallel encoding ....................................... 16
    Description ................................................. 16
    Use cases and benefits .................................... 18
  9.6.5 Tag Power Indicator .................................. 18
    Description ................................................. 18
    Use cases and benefits .................................... 19
9.6.6 Product Status Flag (PSF) ............................. 20
  9.6.6.1 Description ........................................ 20
  9.6.6.2 Use cases and benefits ............................ 20
10 Limiting values ............................................. 21
11 Characteristics .............................................. 22
  11.1 UCODE 7m bare die characteristics .................. 22
12 Package outline ............................................. 23
13 Packing information .......................................... 23
  13.1 Wafer ..................................................... 23
14 Abbreviations ............................................... 23
15 References ................................................... 24
16 Revision history .............................................. 26
17 Legal information ............................................ 27
  17.1 Data sheet status ........................................ 27
  17.2 Definitions ............................................... 27
  17.3 Disclaimers .............................................. 27
  17.4 Trademarks ............................................... 28
18 Contact information .......................................... 28
19 Contents .......................................................... 29